Simulation of Resonance Reduction In PCBs Utilizing Embedded Capacitance

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IPCWorks 2005- Las Vegas, NV

OAK-MITSUI TECHNOLOGIES
MITSUI KINZOKU CORPORATE GROUP
MITSUI KINZOKU



INTRODUCTION

- Buried Capacitance Drivers
- Material Properties
- PCB Manufacturing Processes
- Impedance/Noise Measurements
- Simulation Results
- Further Studies
- Conclusion



Background / Motivation

High speed computing boards

Servers, Routers, Super computers

CPU processor speed ↑
Operation voltage ↓
Power consumption ↑

Power distribution improvement

Embedded capacitor

Module boards

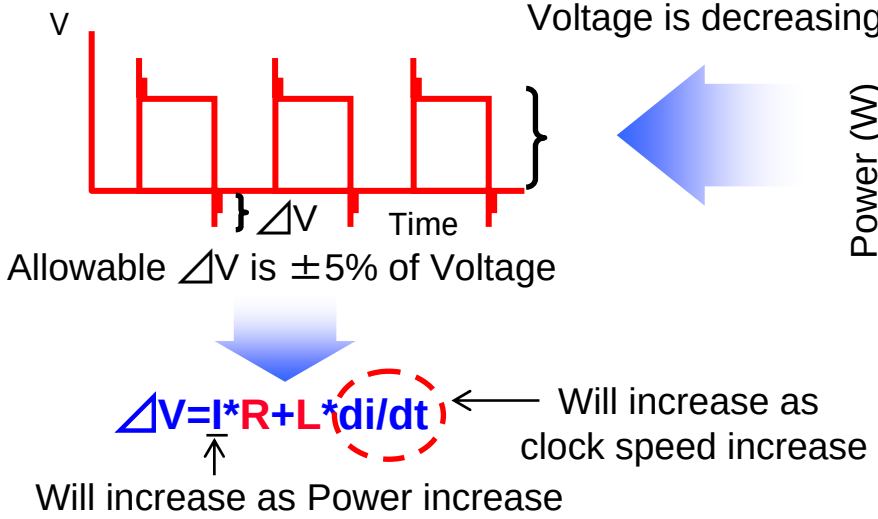
Cell phones, PDA, Note book computers

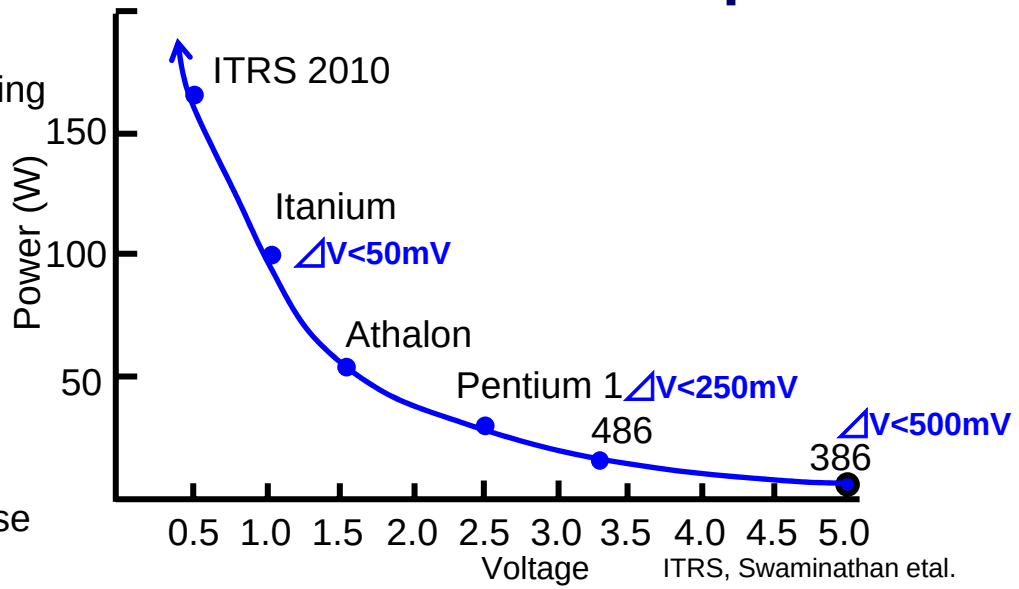
Multiple band ↑
More functions ↑
Cost ↓

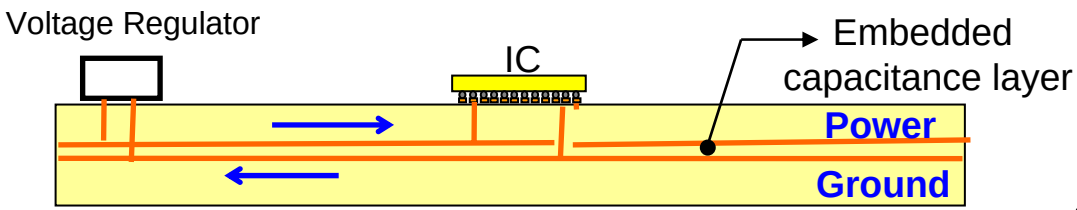
Miniaturization / HDI

Embedded capacitor

Background of demand for PCB with Embedded Capacitor





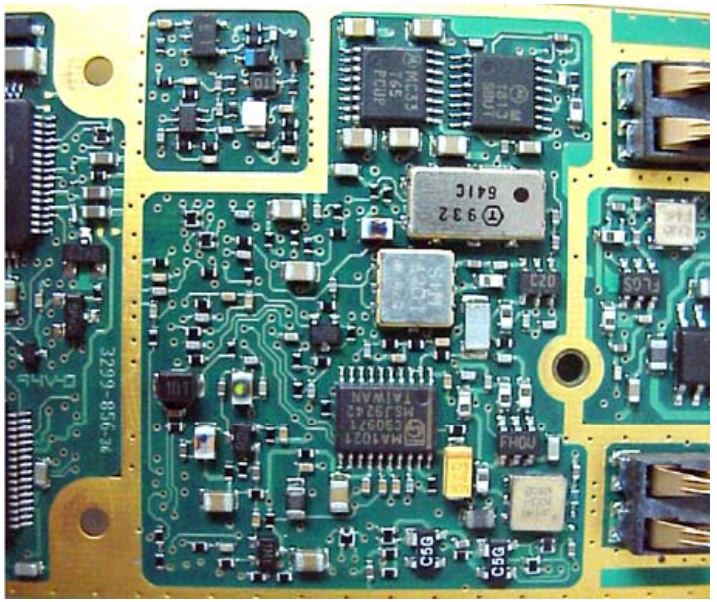


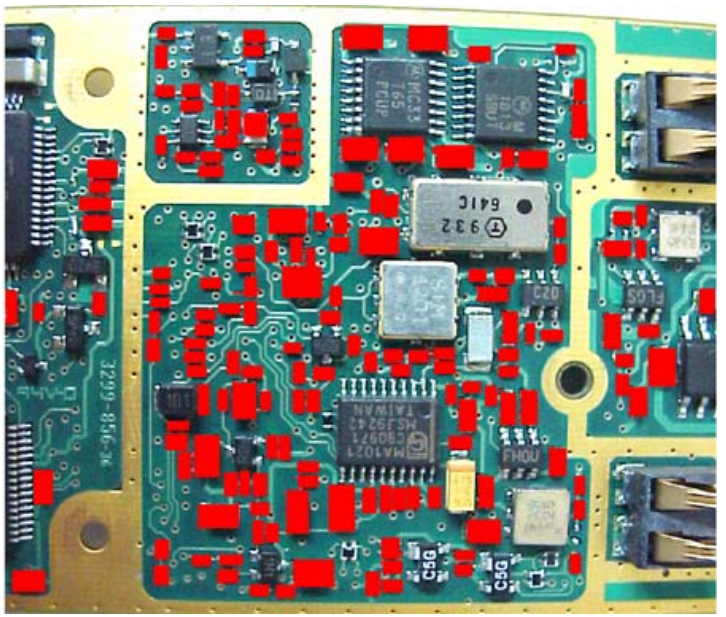
L∝Loop area ∝Power ground thickness

"Thin" power ground plane is the key parameter to improve electrical performance at high frequency!

Background of demand for PCB with Embedded Capacitor

Component density is reaching its limit





Passive components

Source: Richard Ulrich University of Arkansas

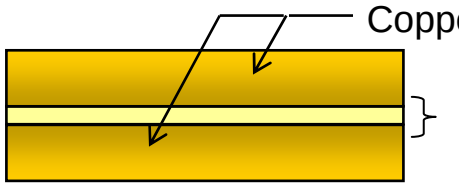
High capacitance and capacitance uniformity is the key to embed

Solution

High speed computing boards
Servers, Routers, Super computers

Power distribution improvement

Uitra-Thin substrate
for use as embedded capacitor

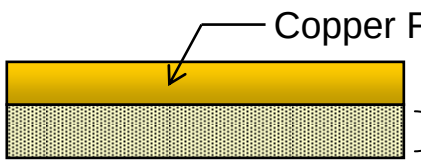


8～24 micron Polymer Dielectric

Module boards
Cell phones, PDA, Note book computers

Miniaturization / HDI

Hi-Dk RCF
for used as embedded capacitor

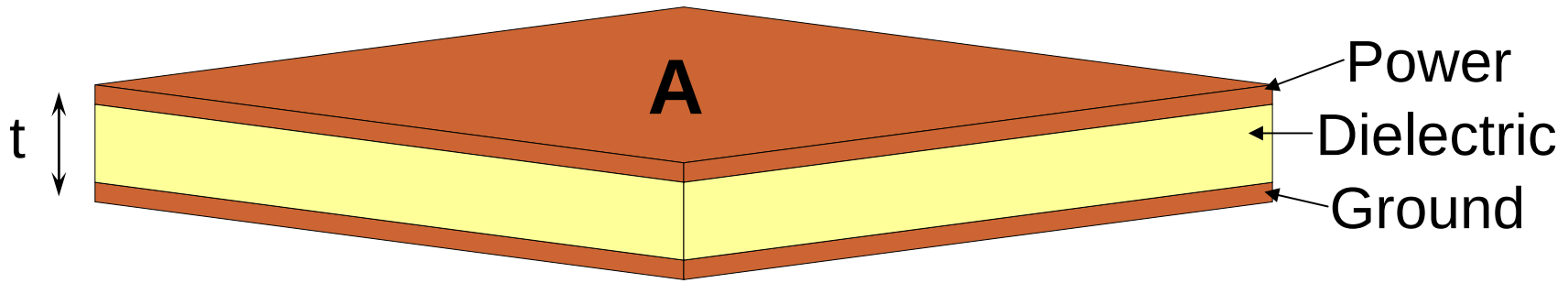


16 micron Polymer Dielectric with Hi-Dk Filler

Note: Manufacturing and use of Distributed (planar) Capacitance requires review of existing patents in the field including those of Sanmina-SCI.

Product Design

Planar Capacitor



$$C = \frac{A * D_k * K}{t}$$

Where:

C = Capacitance (Farads)

A = Area of plates

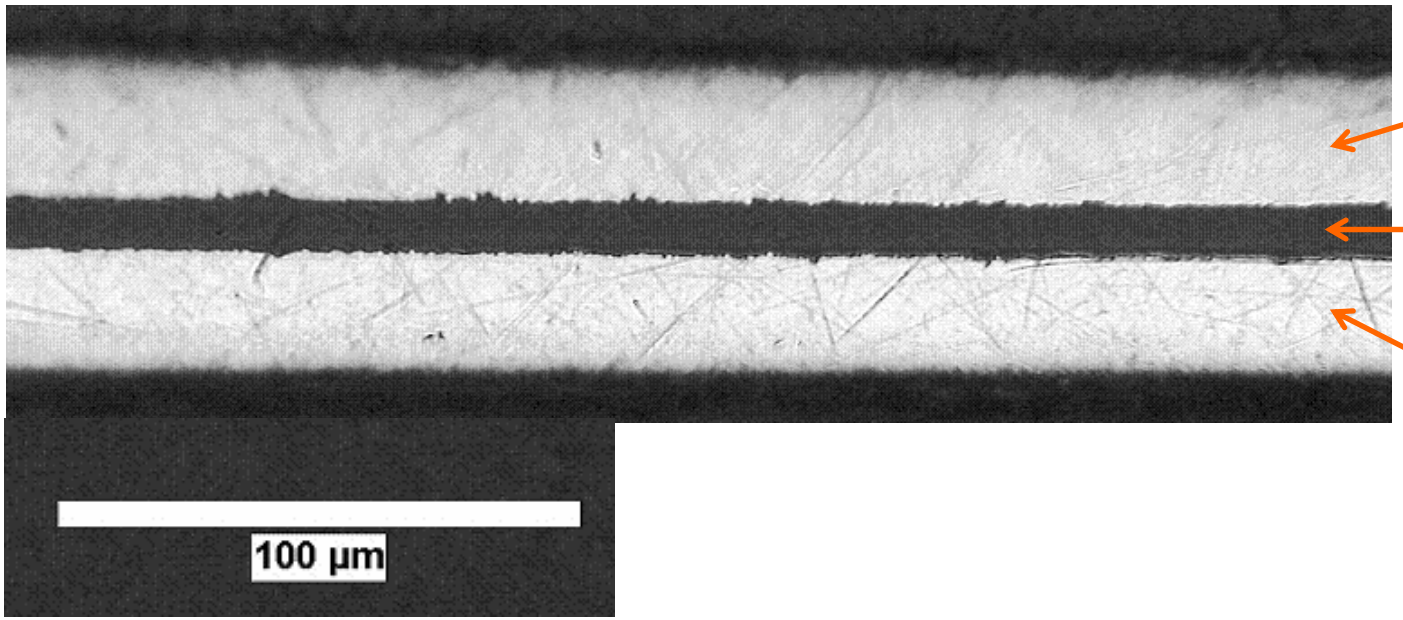
D_k = Dielectric constant of material between plates

K = Constant

t = Thickness between plates

Ultra-Thin substrate for use as power distribution layer

Construction of ultra-thin substrate



Embedded Capacitor Material Characteristic data

Properties	Method						
	IPC or others	BC24	BC16	BC12	BC8	BC12TM	BC16T
Dielectric Thickness, µm	Nominal	24	16	12	8	12	16
Cp@ 1MHz, nF/in^2(pF/cm^2)	IPC TM-650 2.5.5.3	**1.0 (155)**	**1.6 (250)**	**1.9 (300)**	**3.1 (480)**	**4.5 (700)**	**11 (1700)**
Dk @1Mhz	IPC TM-650 2.5.5.3	4.4	4.4	4.4	4.4	10	30
Loss Tangent @ 1 MHz	IPC TM-650 2.5.5.3	0.015	0.015	0.015	0.016	0.019	0.019
Peel Strength, lbs/in	IPC TM-650 2.4.9	>8	>8	>8	>8	>4	>6
Dielectric Strength, kV/mil	IPC TM-650 2.5.6.3	5.3	7.3	5	5	6.2	2.8
Tensile Strength, Mpa (kpsi)	ASTM D-882A	152(22.0)	164(23.8)	194(28.2)	126(18.3)	110(16.0)	NA
Elongation, %	ASTM D-882A	18.5	16.5	11.5	8.5	6.0	NA
CTE, ppm/^{o}C x-y d(20-100^{o}C)/ (100-200^{o}C)	TMA	14 / 23	14 / 23	14 / 23	16 / 28	16 / 38	NA
Boil test, 2hrs Boil in water, 20 sec dip @260C solder (10spec)	-	Pass	Pass	Pass	Pass	Pass	Pass
Thermal Stress (20Sec Float @288C), Times	-	>10	>10	>10	>10	>10	>10
Migration, 85C/85%RH/DC 35V	-	>1000	>1000	>1000	>1000	>1000	>1000
Flammability/Temp Rating	UL-94/ UL746	V0 130^{o}C	V0 130^{o}C	V0 130^{o}C	V0 130^{o}C	Pending	Provisional
PWB Processing	-	Both side etching	Both side etching	Both side etching	Both side etching	Both side etching	Sequential Lamination

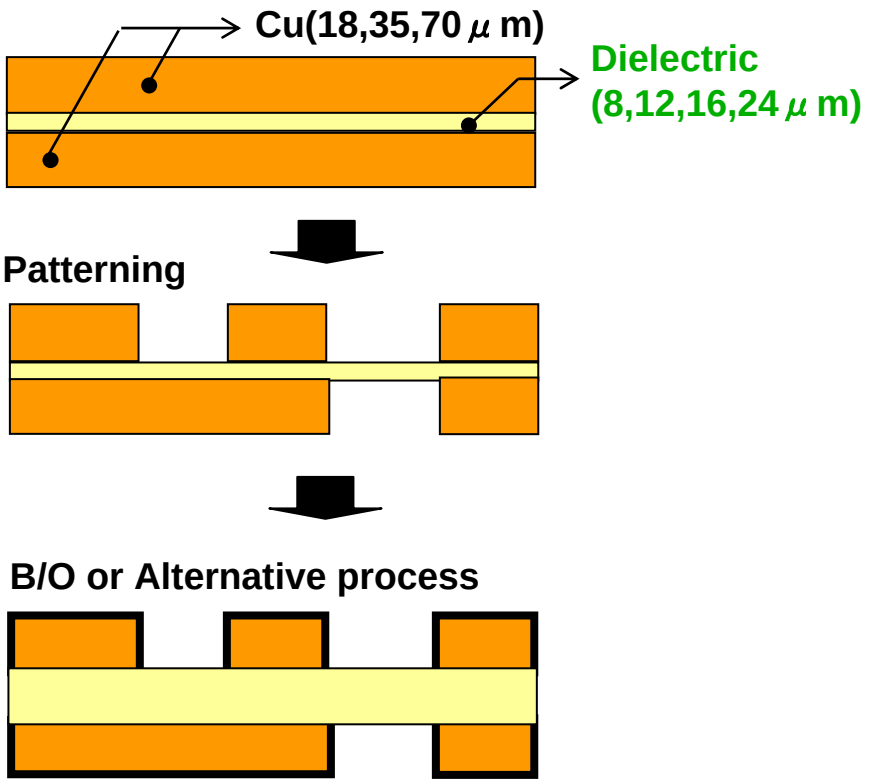
NA=Not Applicable

Processing guideline

1. **Pre-clean**
   - Standard process
2. **Expose Image**
   - Standard process
3. **Dry Film lamination**
   - Standard process

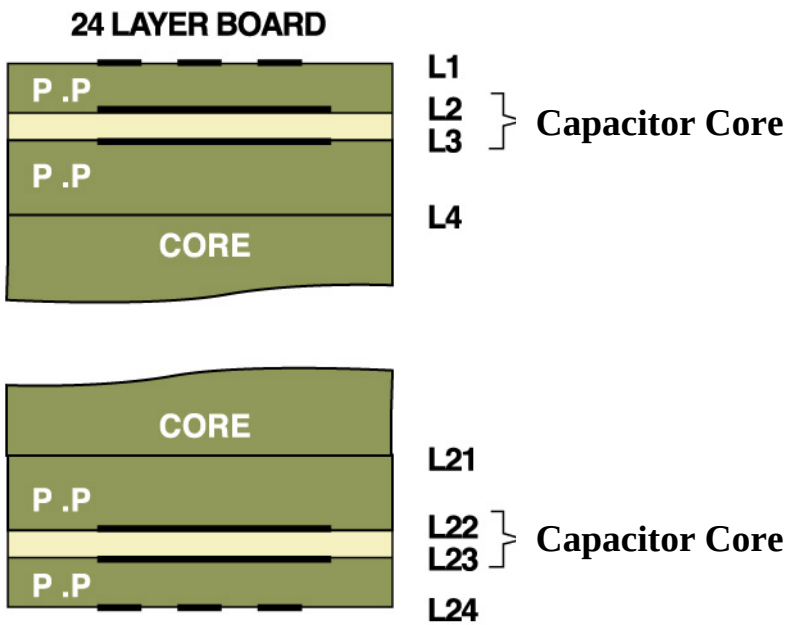
4. **Pattern etching**
   - Thin core compatible line recommended
     Ex) Thin core Schmid etching line
   - Use leader board if not confident
   - Careful Handling required
5. **Black oxidizing or alternative oxides**
   - Thin core compatible line recommended
   - Use leader board if not confident
   - Horizontal line preferred
   - Careful Handling required

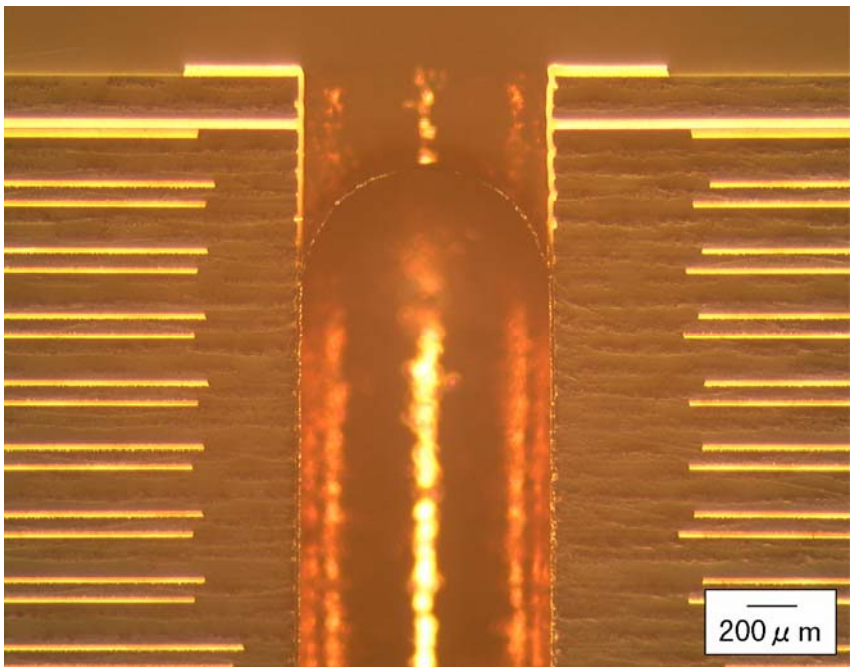
Important



PCB Example

24 Layer Board





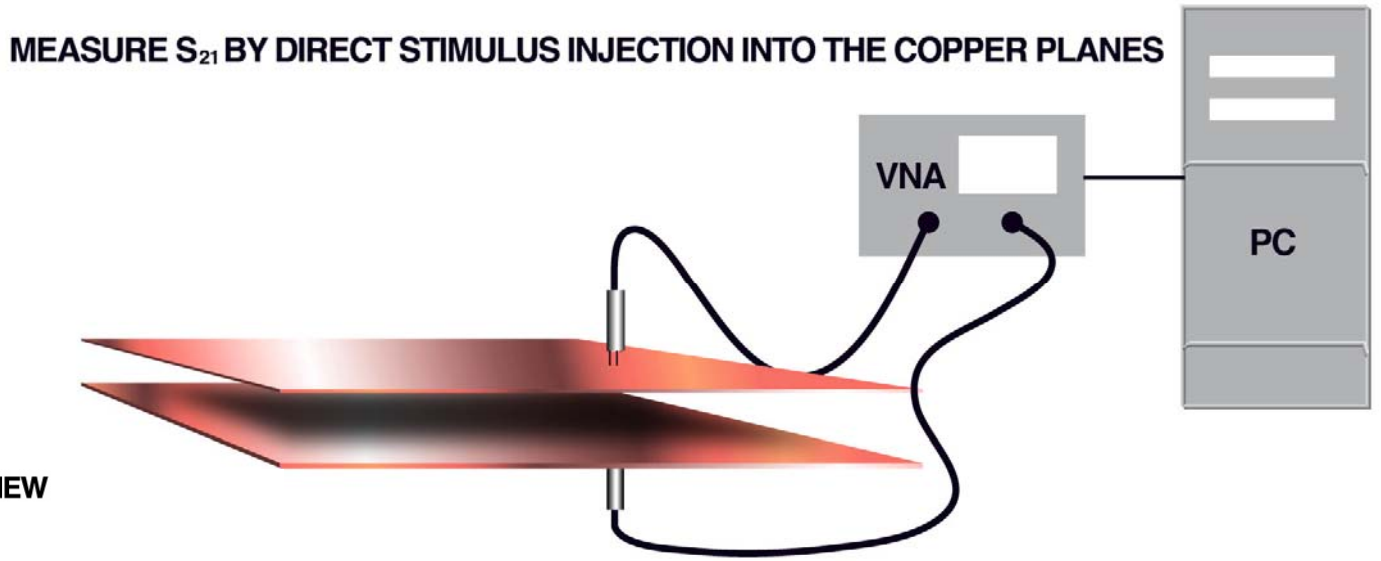
}12 μm

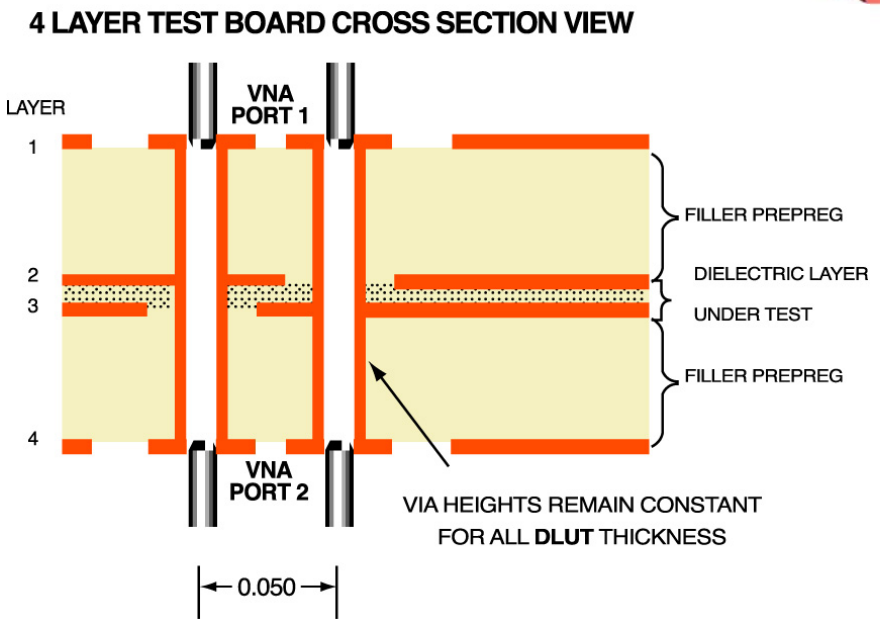
Reliability Tests

Description	
6x Through Hole Solder Shock	**PASS**
6x Blind Via Solder Shock	**PASS**
Dielectric Thickness per Cross Section within +/-10%	**PASS**
T-260(>5min)	**PASS**
IST Testing (500 cycles)	**PASS**
Core Level Hi-Pot Testing 100Cores(100V/sec; 500Vmax)	**PASS**
Finished Circuit Level Hi-Pot 50 circuits (100V/sec; 500Vmax)	**PASS**

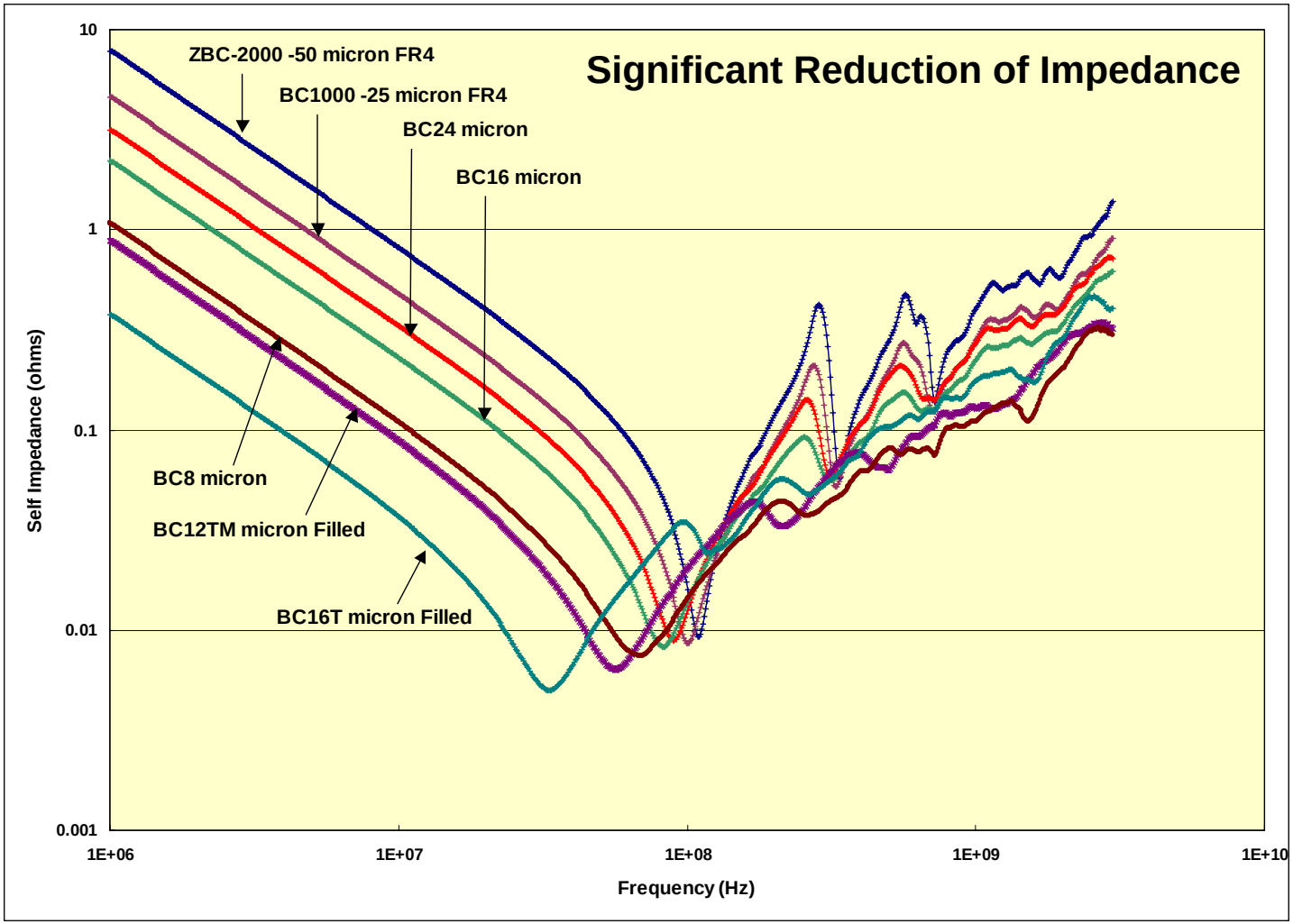
Courtesy of Sanmina-SCI

PCB Electrical Performance





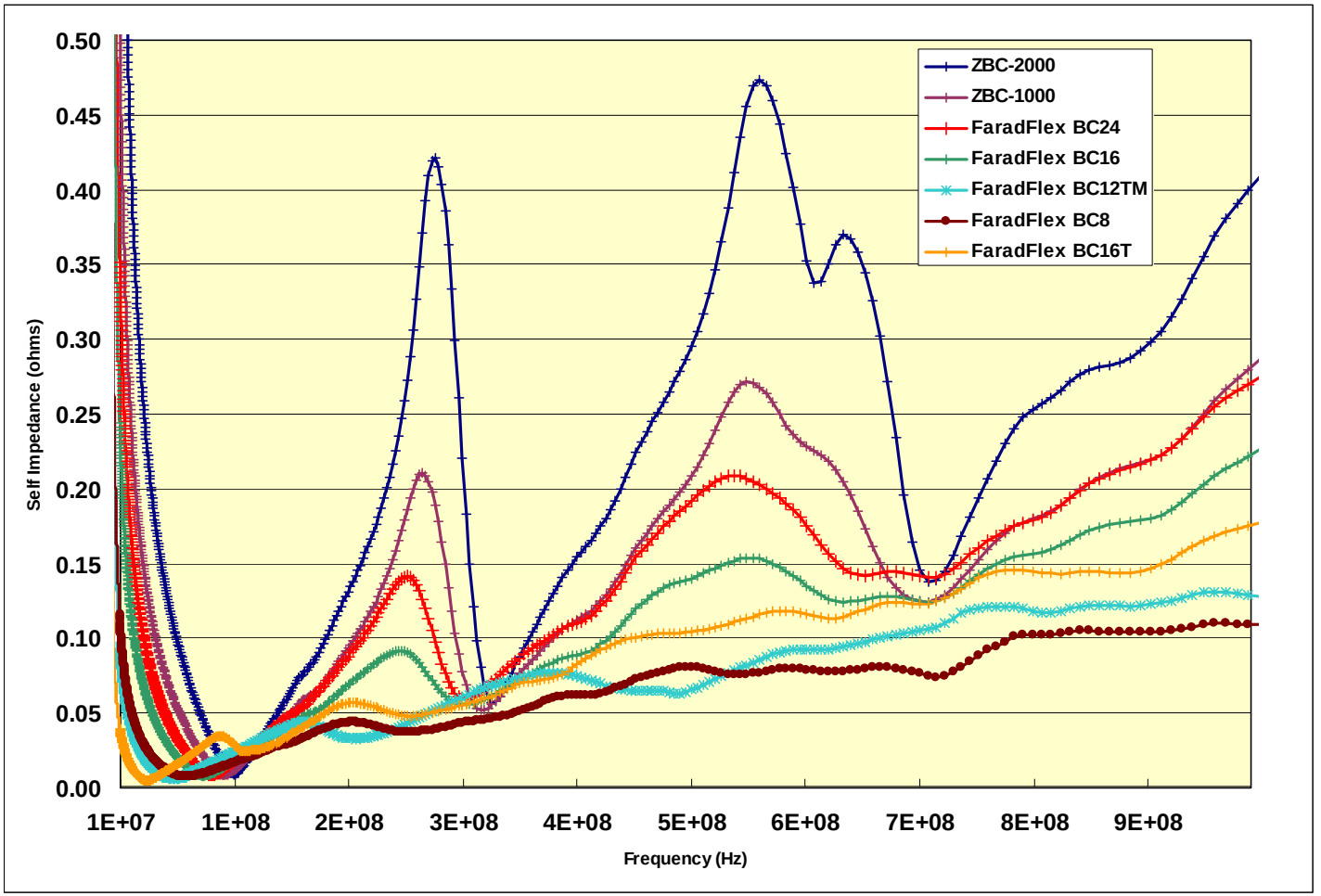
PCB Electrical Performance



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

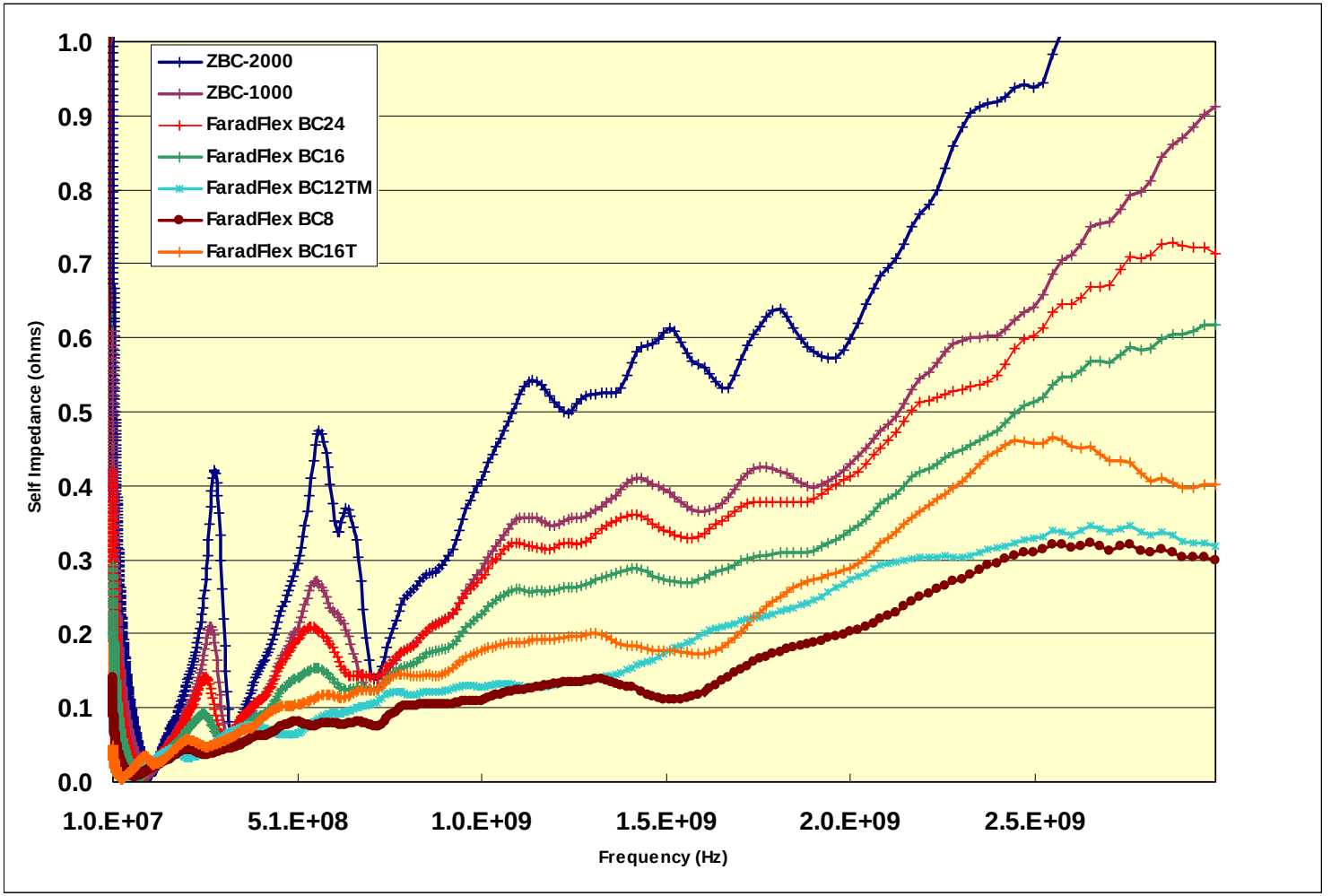
PCB Electrical Performance (Up to 1 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

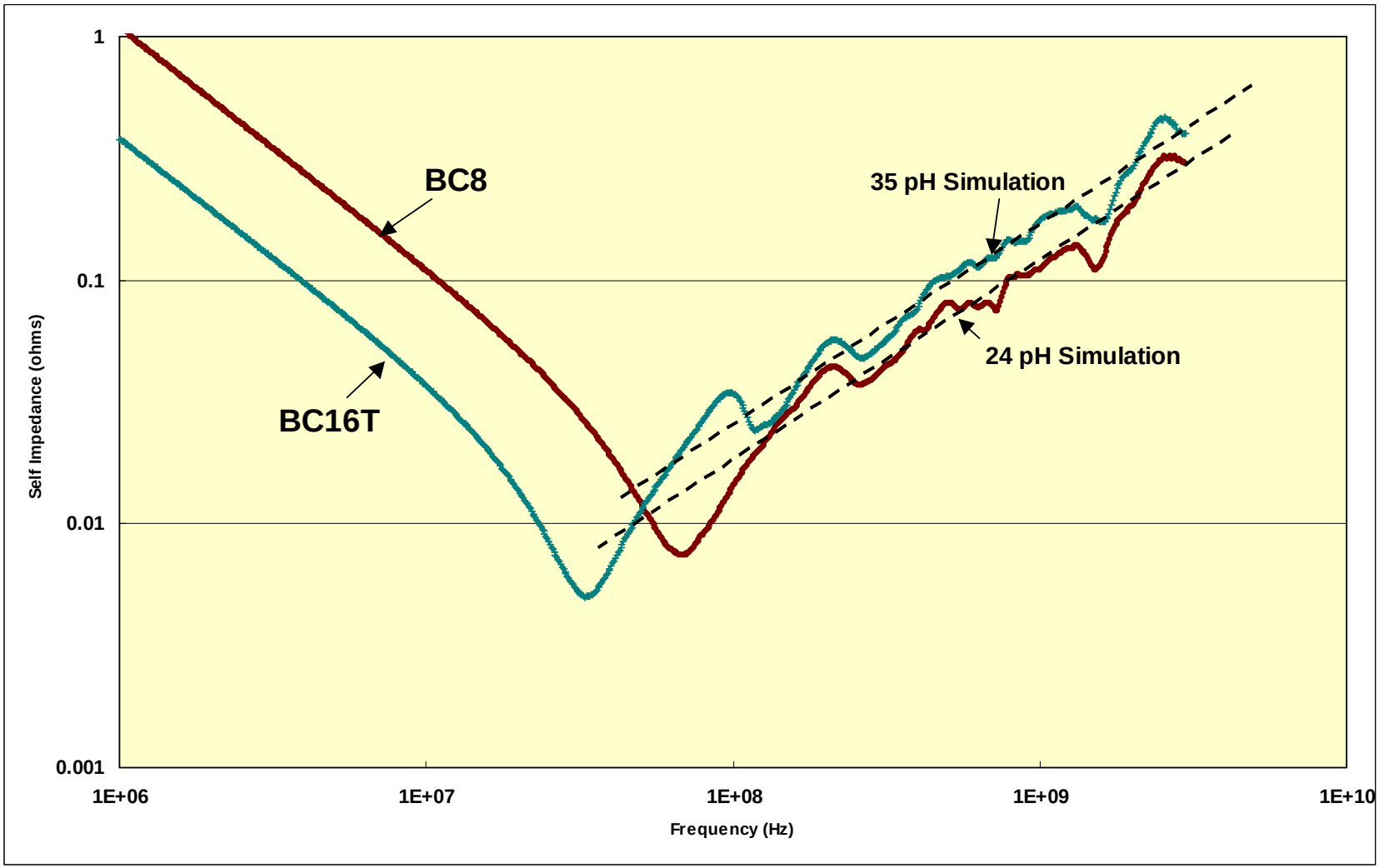
PCB Electrical Performance (Up to 3 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

PCB Electrical Performance (Thin versus High Dk)



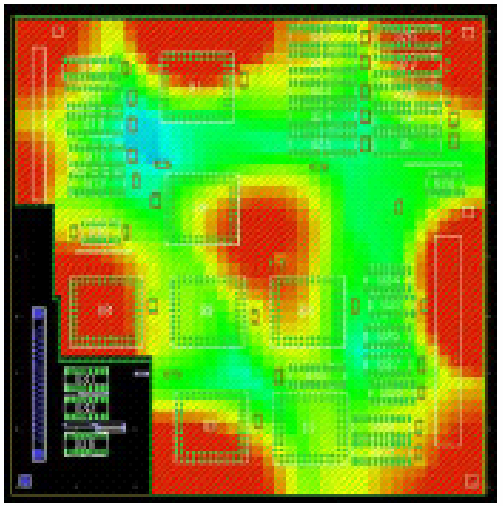


Power/Ground Plane Simulation

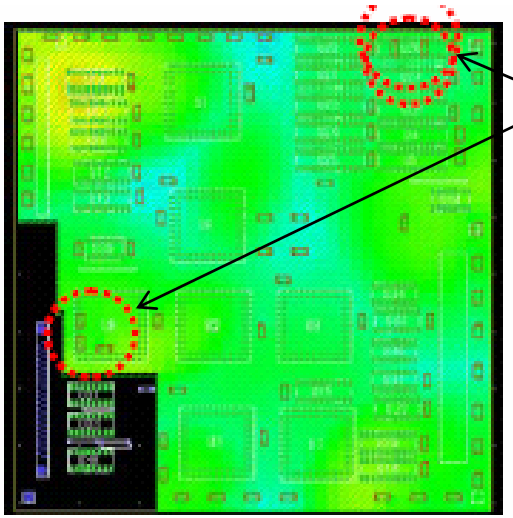
- Utilize EMI Stream
  - Developed by NEC
  - Based on SPICE Model
- Input PCB Layout in Design Format (.dsn file)
  - Output provide by standard design tools (Mentor Graphics, Cadence, etc.)
- Select thickness, Dk and Cu thickness of P/G planes
- Select frequency range
- Can add/subtract discrete SMT capacitors

Resonance Distribution

35- 0.1µF caps
for power supply



0dB

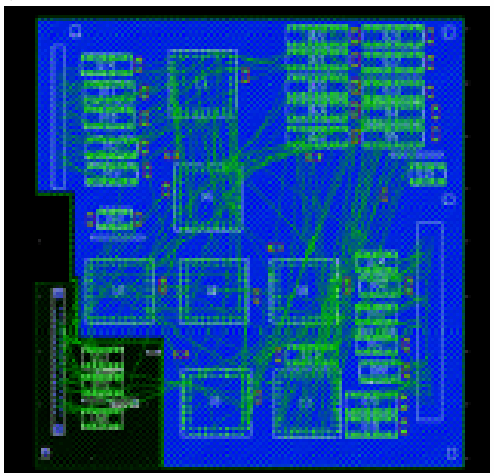


Can not place caps!

35- 0.1µF caps
for power supply
+44-0.1 µF caps
for resonances

0.4mm (16 mil P/G)

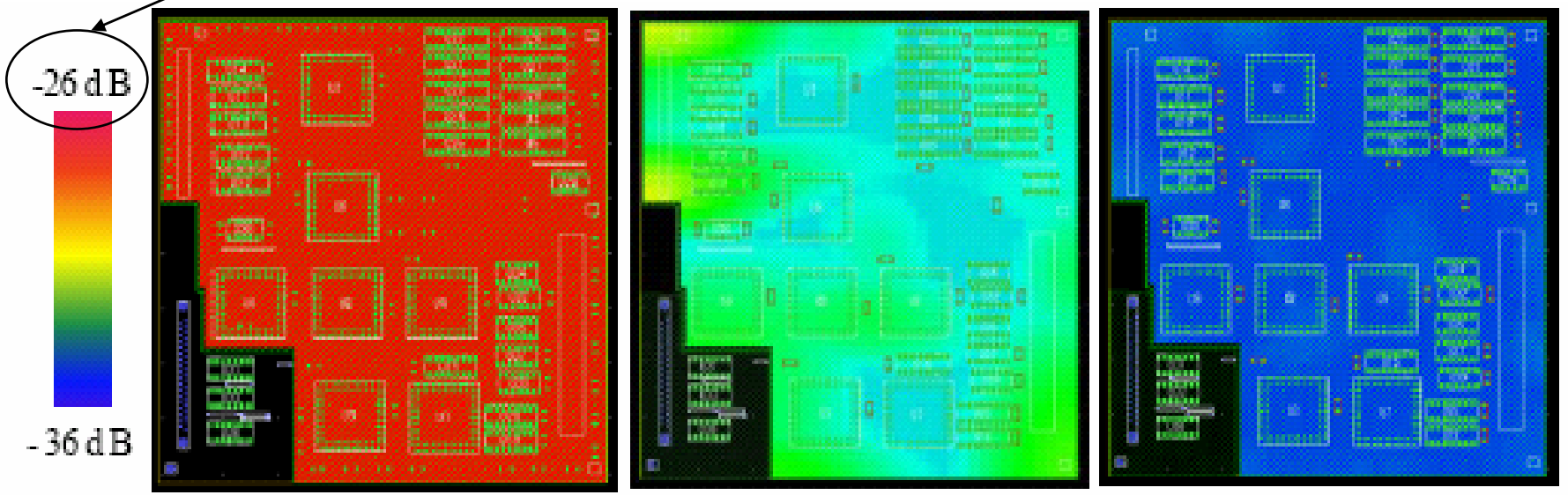
24 µm P/G
Dk 4.4
No additional caps



0dB

Simulations provided by TechDream, Inc.

Resonance Distribution- Lower Noise Threshold

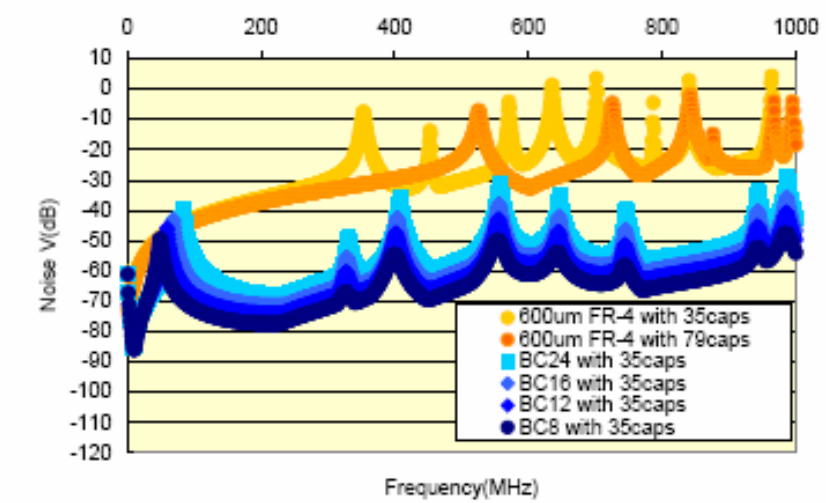


400 µm (16 mil P/G)
79 caps

24 µm P/G
Dk 4.4
35 caps

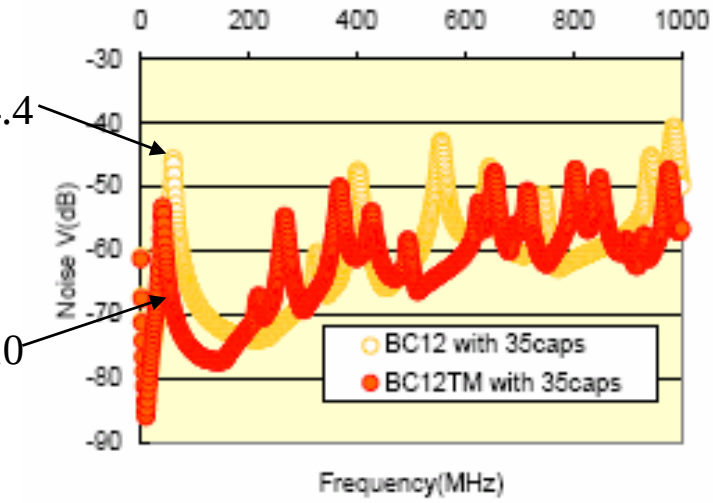
12 µm P/G
Dk 10
35 caps

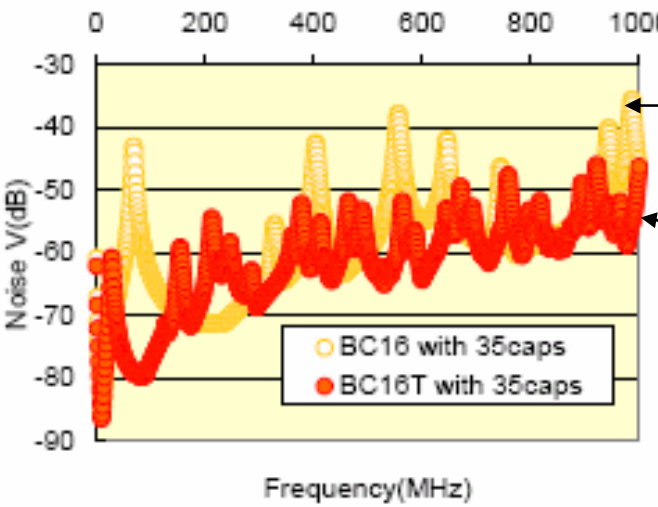
Frequency Response- Effect of Thickness, Dk



Dk-4.4

Dk-10



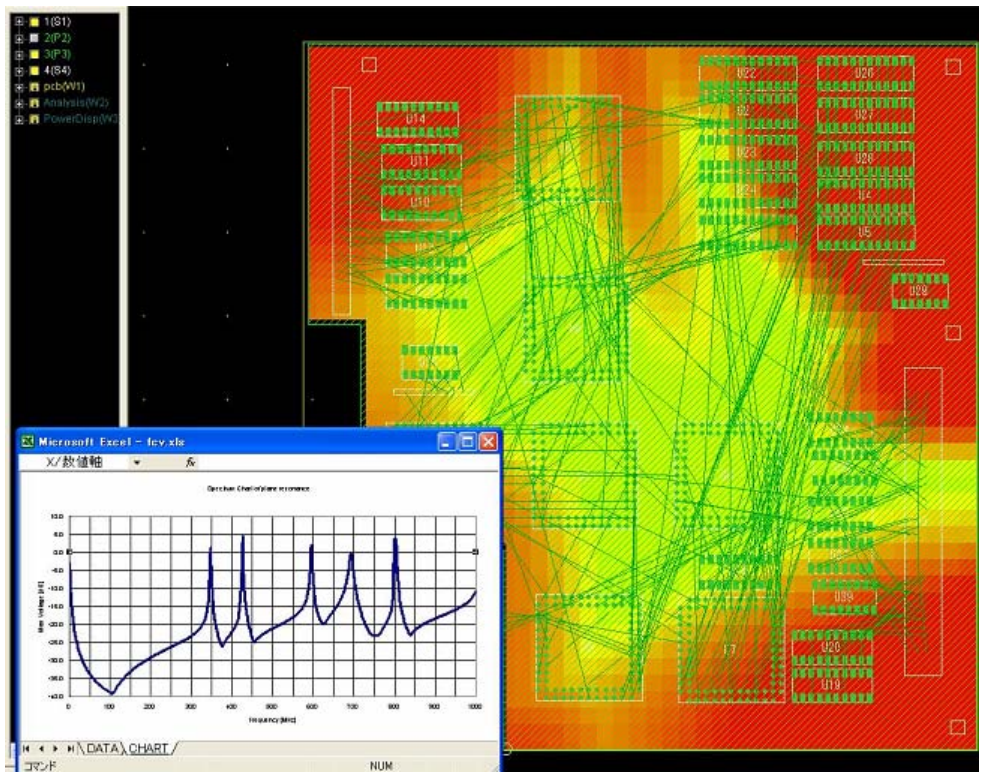


Dk-4.4

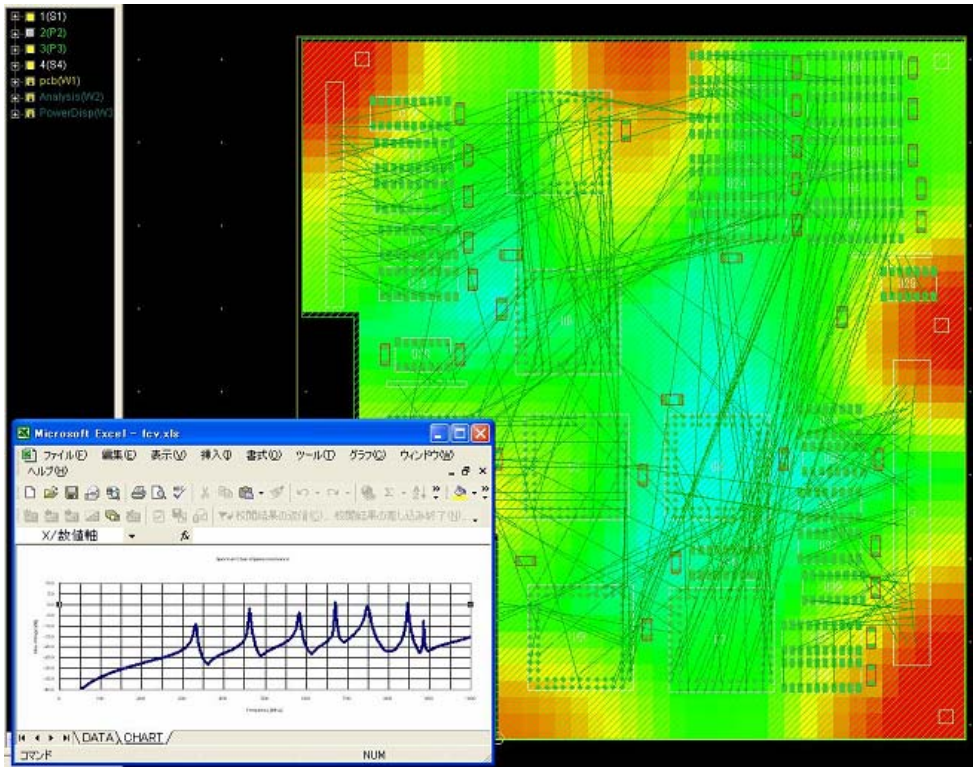
Dk-30

Test Board –Simulation #2

Standard core(400umFR-4) with no caps

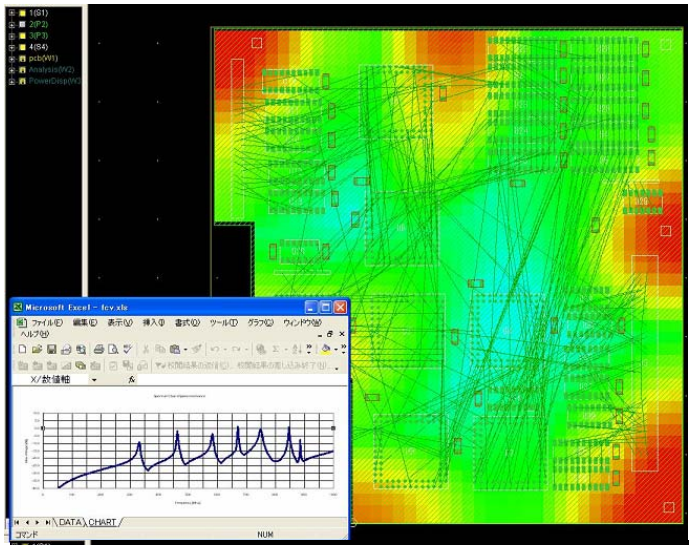


Standard core(400umFR-4) with caps

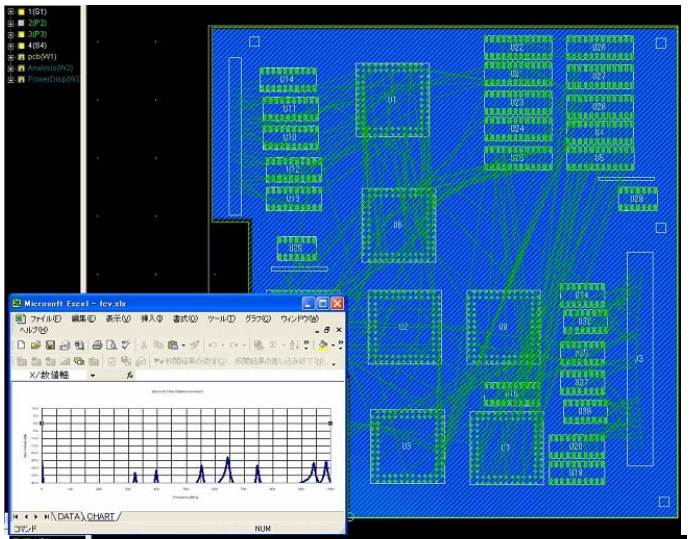


Test Board- Simulation #2

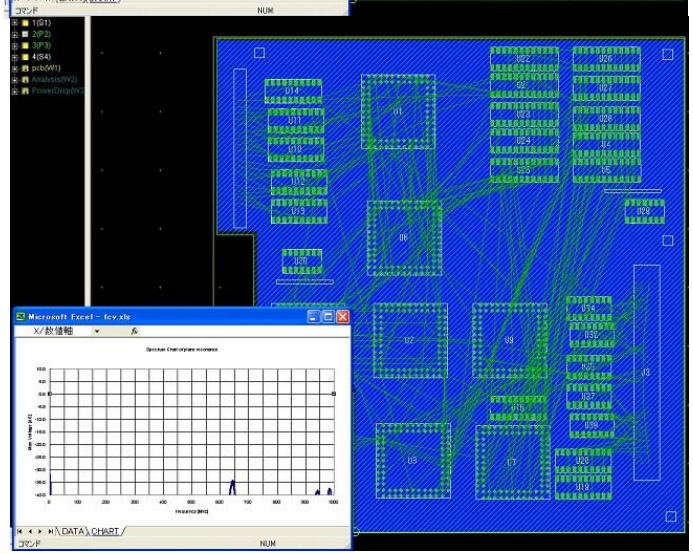
P/G Plane
FR-4 400um
With Caps



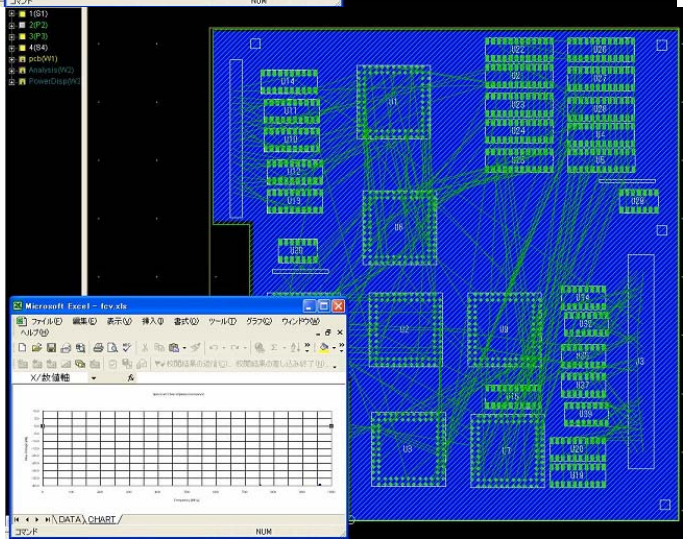
P/G Plane
BC24

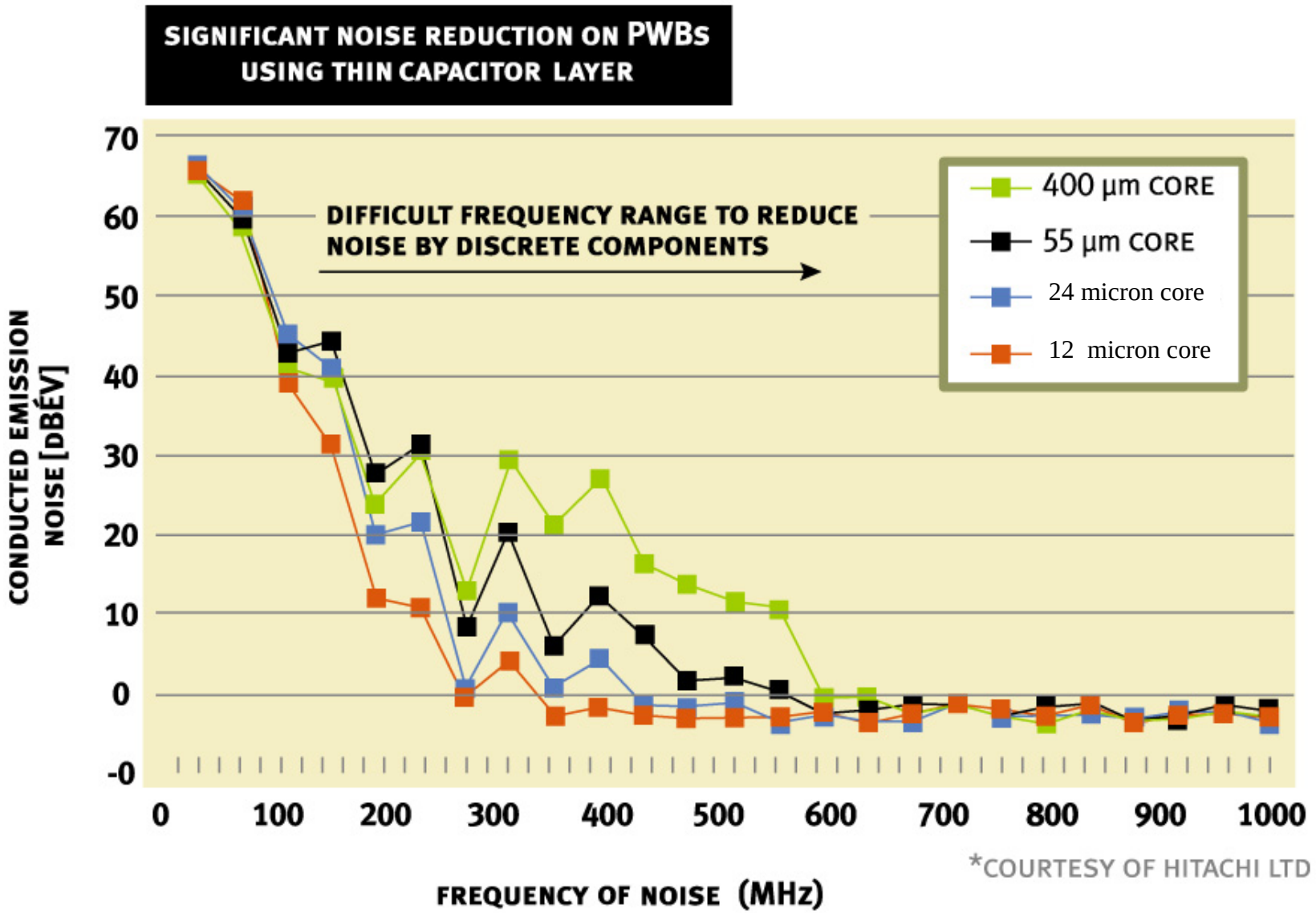


P/G Plane
BC12



P/G Plane
BC16T




SIGNIFICANT NOISE REDUCTION ON PWBs
USING THIN CAPACITOR LAYER
DIFFICULT FREQUENCY RANGE TO REDUCE
NOISE BY DISCRETE COMPONENTS
400 µm CORE
55 µm CORE
24 micron core
12 micron core
CONDUCTED EMISSION
NOISE [dBÉV]
70
60
50
40
30
20
10
0
-0
0
100
200
300
400
500
600
700
800
900
1000
FREQUENCY OF NOISE (MHz)
*COURTESY OF HITACHI LTD



Process Flow for Embedded Distributed Capacitance

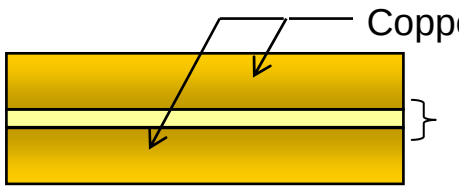
- Select PCB Design as Candidate
  - Know problem with P/G noise, EMI
  - High pF Capacitor density
- Provide .dsn file for Simulation
- Set-up and run Simulation
- Build Prototype based on Simulation
- Analyze Prototype and Finalize design

Solution

High speed computing boards
Servers, Routers, Super computers

Power distribution improvement

Ultra-Thin substrate
for use as embedded capacitor

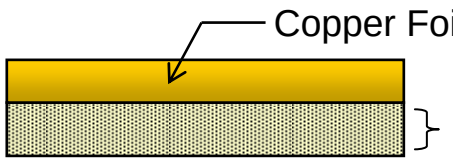


8～24 micron Polymer Dielectric

Module boards
Cell phones, PDA, Note book computers

Miniaturization / HDI

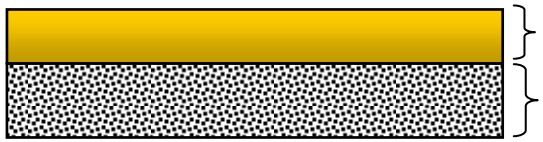
Hi-Dk RCF
for used as embedded capacitor



16 micron Polymer Dielectric with Hi-Dk Filler

Note: Manufacturing and use of Distributed (planar) Capacitance requires review of existing patents in the field including those of Sanmina-SCI.

Hi-Dk RCF Material Construction



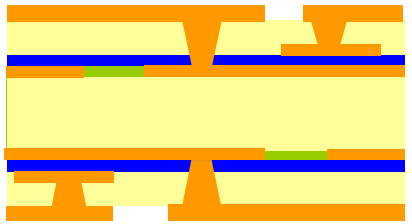
Copper Foil

16 micron Polymer Dielectric with Hi-Dk Filler

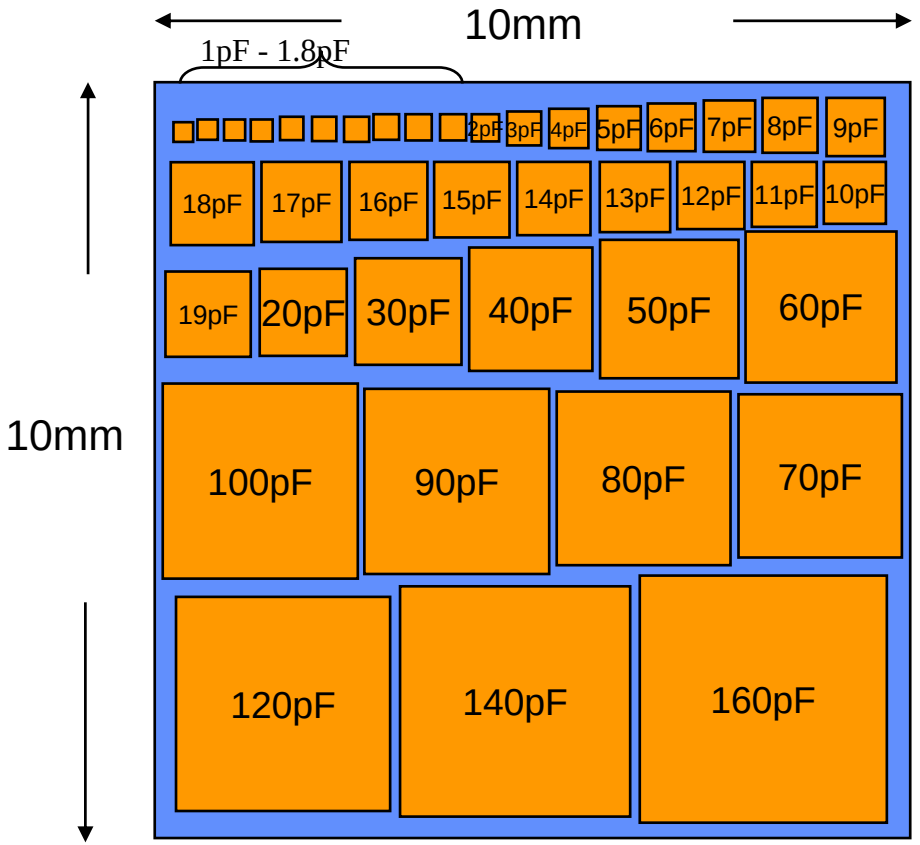
Characteristics	Condition	Unit	*BC16TR*
Capacitance	1MHz	pF/cm^2	1,700
Dk	1MHz	N/A	30
Df	1MHz	N/A	0.019
Dielectric Thickness	Nominal	Micron Meter	16
Peel Strength	IPC TM-650 2.4.9	kN/m	>0.7
Thermal Stress	20sec @288C	times	>10
Electrical Migration	85C/85%RH/ 35V	hrs	>1000

Designing Embedded Capacitance Board

Geometry and Capacitance(Example)



40 capacitors ranging from 1pF to 160pF in 10x10mm



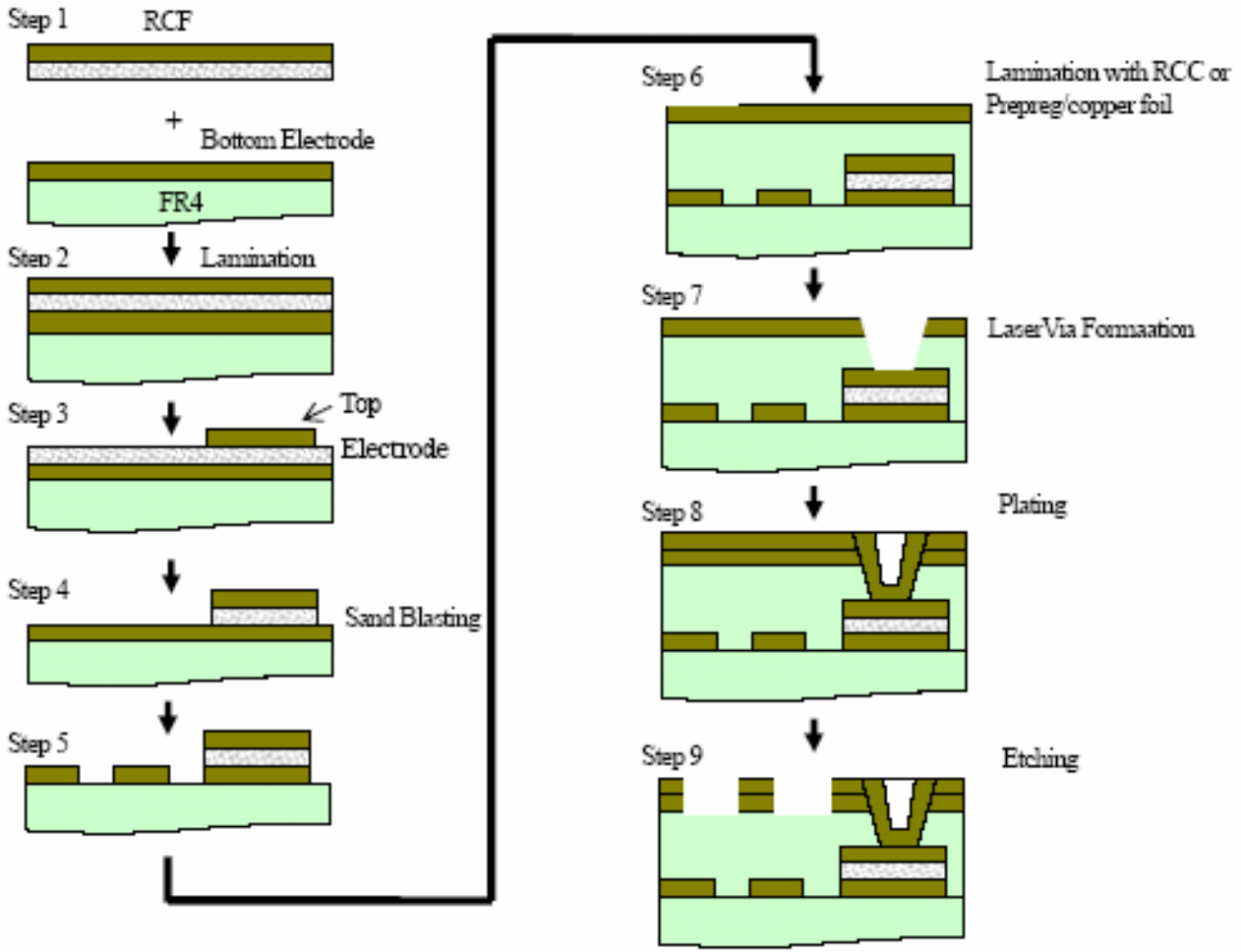
Expected tolerance*

1 - 2pF	5 - 10%
2 - 10pF	3 - 5%
10 - 20pF	2 - 3%
20 - 100pF	1 -2%
100 -	< 1%

*Based on electrode geometry definition +/- 10micron

Geometry calculated based upon 16µ Filled material: 1,700pF/cm^2

“Discrete” Capacitor Process Using Resin Coated Foil

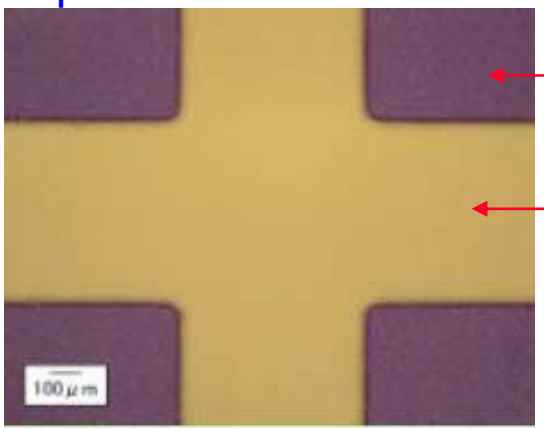


Removal of dielectric layer

Top view

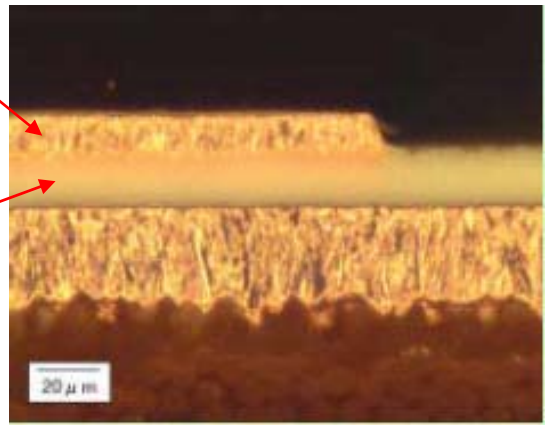
Cross sectional

Before sand blast process

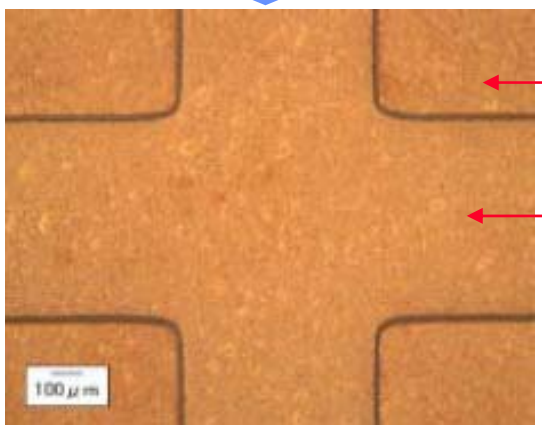


Top electrode

Dielectric layer

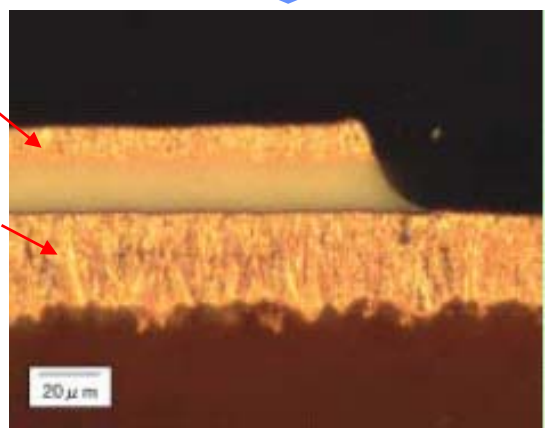


After sand blast process



Top electrode

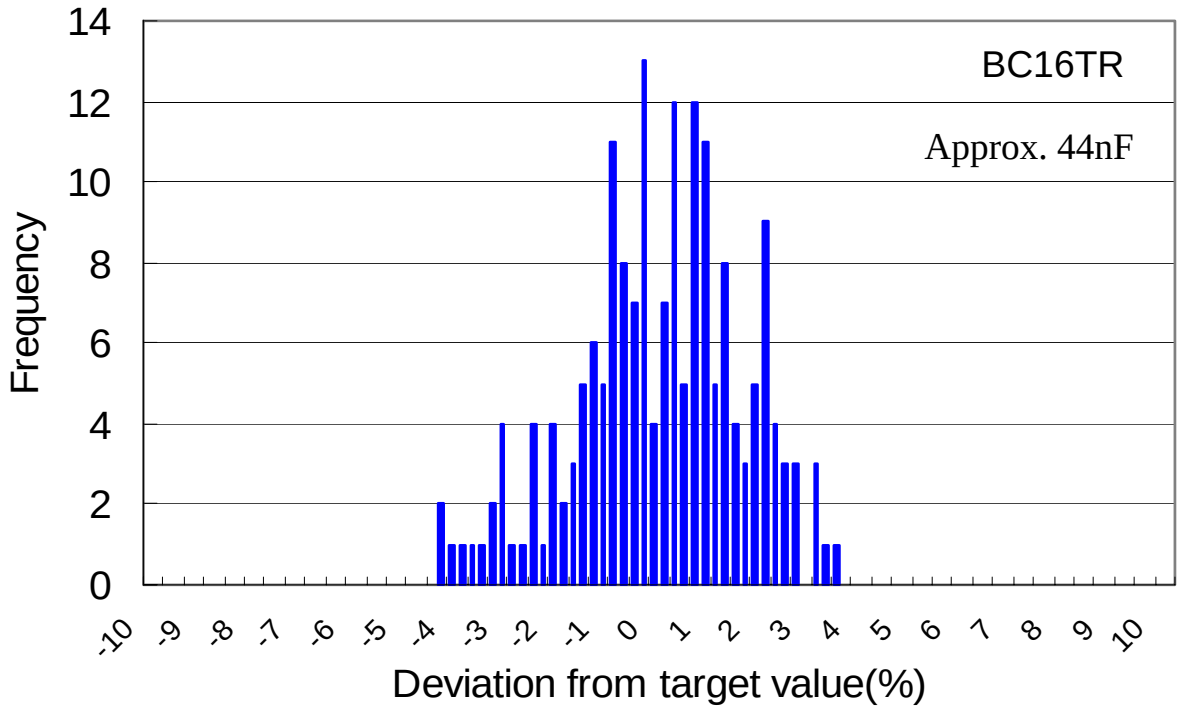
Bottom electrode

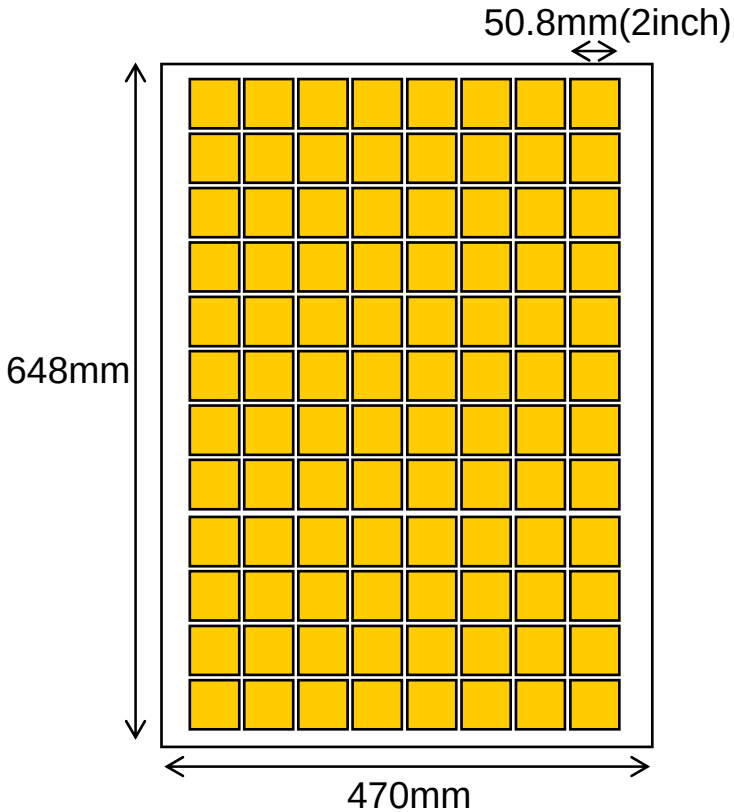


Ishi Hyoki
#A600, 5kg/cm^2

Capacitance uniformity evaluation result

Test 1.



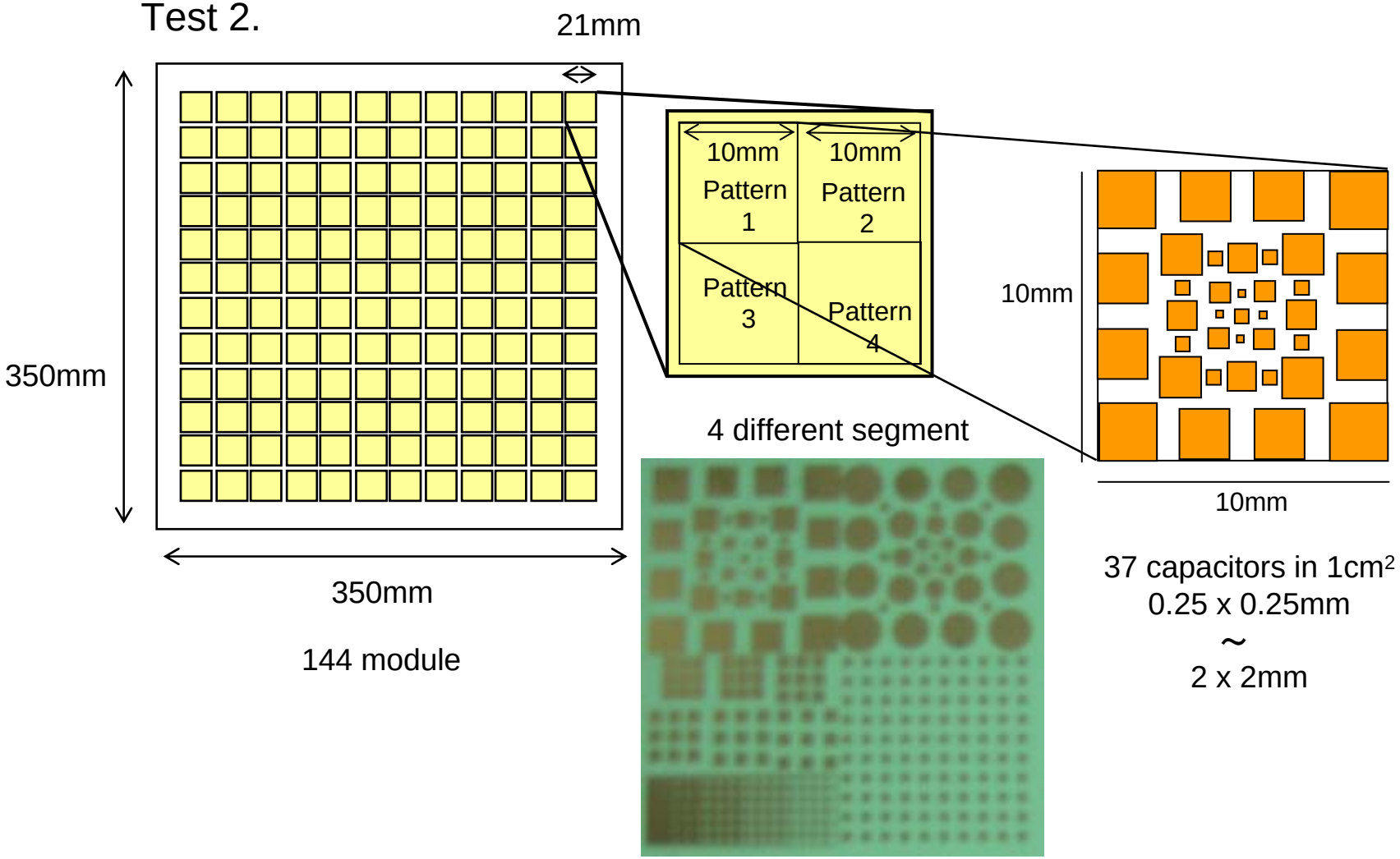


Capacitor size : 50.8x50.8mm
192 measurement points

Uniformity <5%

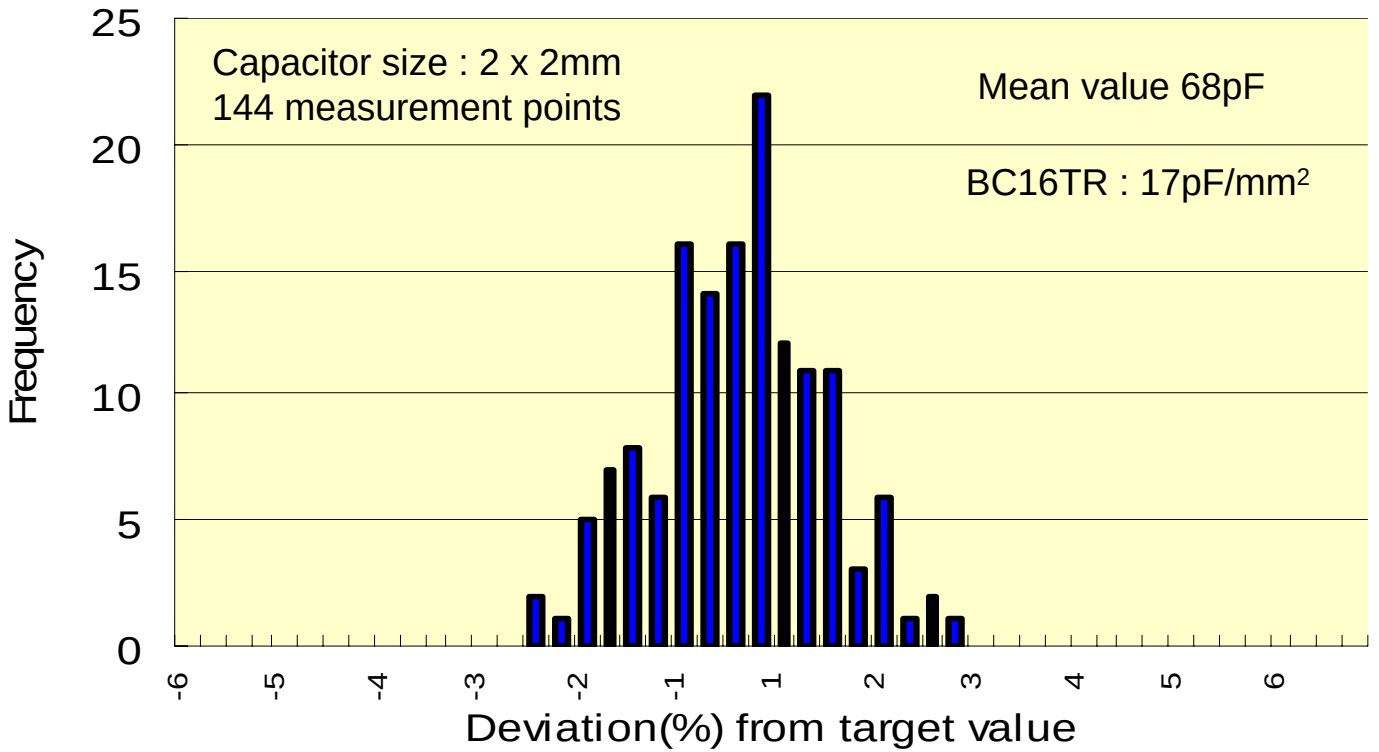
Capacitance uniformity evaluation

Test 2.



Capacitance uniformity evaluation result

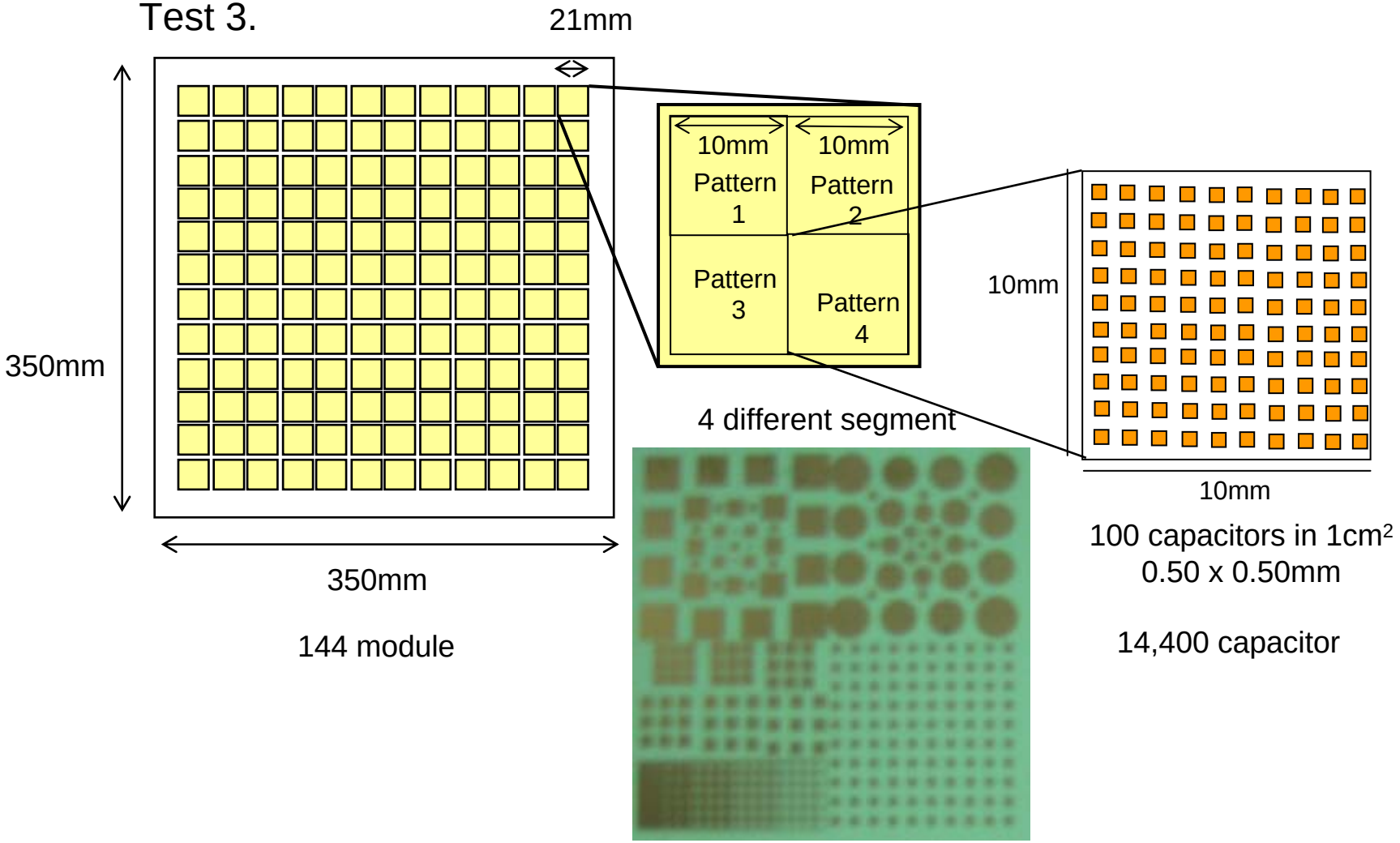
Test 2.



Uniformity <5%

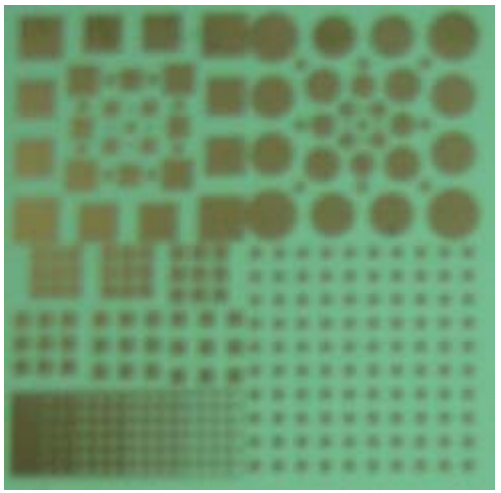
Capacitance uniformity evaluation

Test 3.



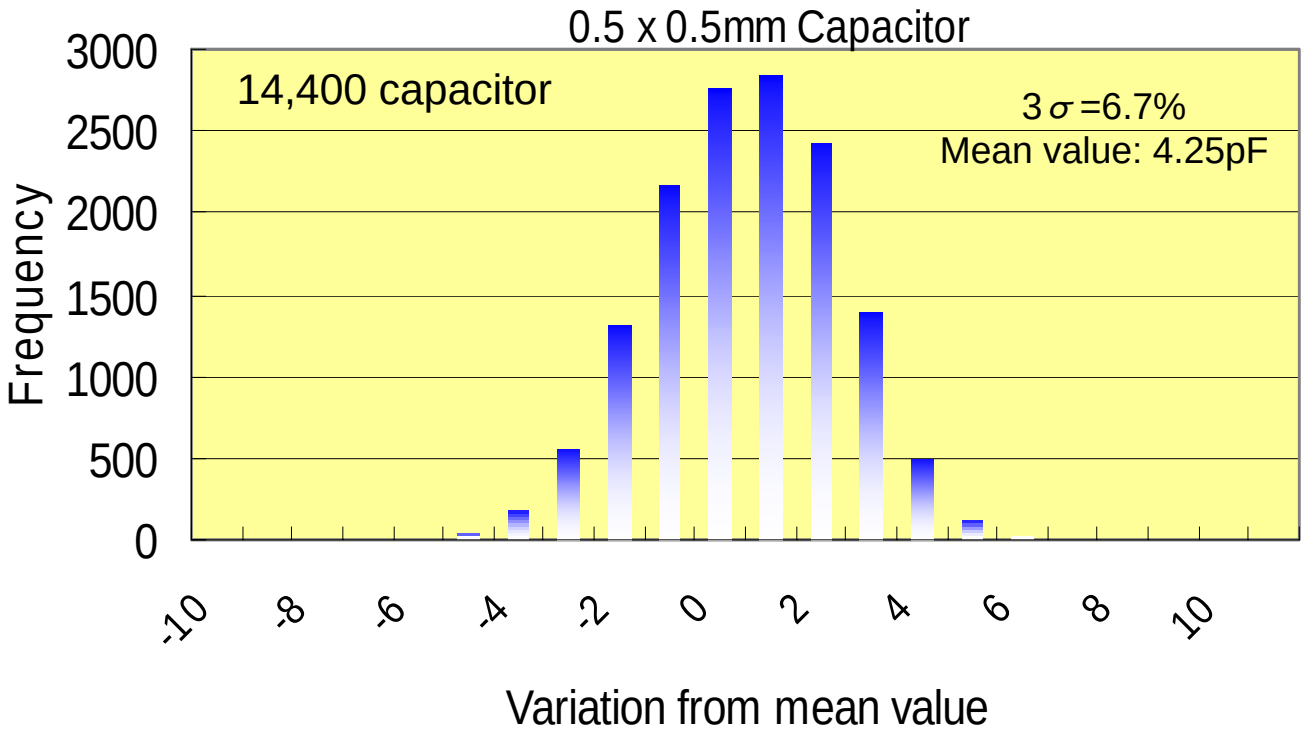
Flying probe LCR measurement of embedded passive Boards





Capacitance uniformity evaluation result

Test 3.



Uniformity <7%



Further Studies

- Measure EMI from assembled boards and compare with Simulation results
- Conduct High Frequency testing on “Discrete” Embedded Capacitors
  - Test Vehicle Designed
  - Utilize Crane NAVSEA Facility
  - Test to 12 GHz



Crane Test Vehicles for High Frequency Testing

Stackup 1 of 2 – Resin Coated Foils

Board Features:

- 6 layers
- Does not require thin-core processing
- .006” laser microvias (Layers 1-2,1-3,4-6,5-6)
- Nelco N4000-13 SI
- .030” thick
- Symmetrical
- 2 capacitive layers
- SMOBC, ENIG

LAYER	TYPE	MATERIAL	THICKNESS
1	SIGNAL	1/2 oz. COPPER	0.7
	PREPREG	N4000-13 SI, 1080	3.0
2	SIGNAL CAPACITOR	RESIN COATED FOIL	*
3	GROUND	1/2 oz. COPPER	0.7
	LAMINATE	N4000-13 SI 106, 7628, 7628, 106	20.0
4	GROUND CAPACITOR	1/2 oz. COPPER	0.7
5	SIGNAL	RESIN COATED FOIL	*
	PREPREG	N4000-13 SI, 1080	3.0
6	SIGNAL	1/2 oz. COPPER	0.7

* 1/2 oz. COPPER FOIL
DIELECTRIC THICKNESS VARIES BY MATERIAL

Stackup 2 of 2 – Thin Core Laminates

Board Features:

- 6 layers
- Requires thin-core processing
- .006” laser microvias (Layers 1-2,1-3,4-6,5-6)
- Nelco N4000-13 SI
- .031” thick
- Symmetrical
- 2 capacitive layers
- SMOBC, ENIG

LAYER	TYPE	MATERIAL	THICKNESS
1	SIGNAL	1/2 oz. COPPER	0.7
	PREPREG	N4000-13 SI, 1080	3.0
2	SIGNAL CAPACITOR	1/2 oz. COPPER DIELECTRIC	0.7 *
3	GROUND	1 oz. COPPER	1.4
	PREPREG	N4000-13 SI, 106	2.3
	PREPREG	N4000-13 SI, 7628	7.3
	PREPREG	N4000-13 SI, 7628	7.3
	PREPREG	N4000-13 SI, 106	2.3
4	GROUND CAPACITOR	1 oz. COPPER DIELECTRIC	1.4 *
5	SIGNAL	1/2 oz. COPPER	0.7
	PREPREG	N4000-13 SI, 1080	3.0
6	SIGNAL	1/2 oz. COPPER	0.7

* DIELECTRIC THICKNESS VARIES BY MATERIAL

NAVSEA WARFARE CENTERS CRANE

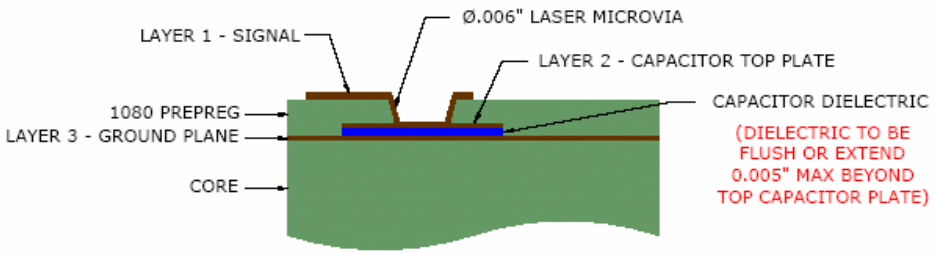
ECIT

Crane Test Vehicles for High Frequency Testing

Capacitor Cross Section 1 of 2

Processing option 1 – Remove the unused capacitor dielectric material

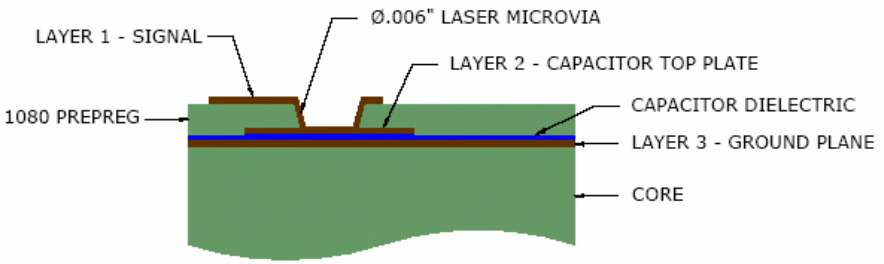
- Capacitor is formed between layers 2 and 3
- Laser microvia connection gives low series inductance



Capacitor Cross Section 2 of 2

Processing option 2 – Unused capacitor dielectric material is not removed

- Capacitor is formed between layers 2 and 3
- Laser microvia connection gives low series inductance



NAVSEA WARFARE CENTERS CRANE

ECIT

Conclusion

- **Embedded Capacitor Technology can Improve System Price/Performance by**
  - **Reducing Discrete Caps**
  - **Reducing PWB size**
  - **Increasing Functionality**
- **Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency**
- **New Substrates have demonstrated *excellent* electrical performance and physical properties.**
- **They are *compatible* with PCB processing; a truly “drop in” material.**
- **Materials are commercially available from Licensed Fabricators**
- **Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PCBs**

Conclusion

- Simulation tools exist to help in determine effectiveness of Embedded Capacitors prior to prototyping.
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- Discrete Capacitors can be formed using High Dk Resin Coated Foil
- Research is being conducted on high frequency response of Embedded “Discrete” Capacitors

Thank You

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Presentation will be available at
www.oakmitsui.com