

OAK-MITSUI TECHNOLOGIES

MITSUI KINZOKU CORPORATE GROUP

MITSUI KINZOKU



FARADFLEX

The drive to increase the speeds and functionality of electronic systems is putting pressure on interconnect designers to supply enough capacitance within the available printed circuit board (PCB) or chip package real estate. They must also reduce impedance, power buss noise and EMI. One way that leading edge designers are accomplishing this is to embed capacitor layers inside the PCB or chip package.

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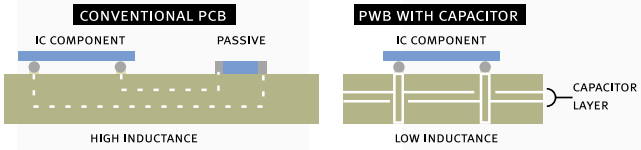
Buried Capacitance™ utilizes the technology of putting a capacitor plane inside the PCB to reduce the overall impedance of the power distribution system, as well as free up surface real estate (by eliminating some discrete capacitors).

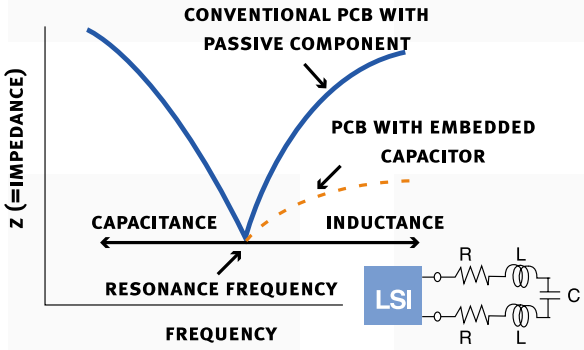
It is the reduced inductance that is a key performance factor in reducing impedance as system frequencies increase.

Fiberglass reinforced epoxy material has been the standard product used to embed these layers in PCBs. These types of substrates have improved the performance of many systems. However, as switching speeds increase, there is a need for even lower impedance power/ground planes.

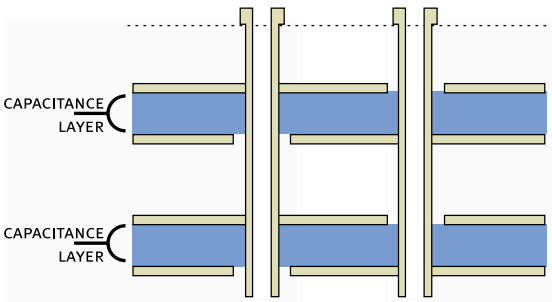
To meet this need, Oak-Mitsui Technologies has developed the FaradFlex™ family of novel thin substrates, that is the next generation of Buried Capacitance™ licensed material.

FaradFlex™ is the *only licensed* polymer film based substrate that can be used when enhanced performance is required over traditional materials. FaradFlex™ provides higher capacitance values and ultra-thin dielectric layer, allowing for significantly lower power/ground plane impedance.

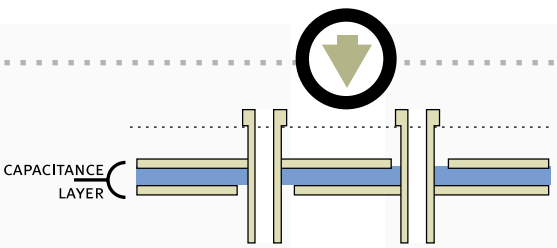




THE NEXT GENERATION OF BURIED CAPACITANCE MATERIAL



CONVENTIONAL MATERIAL
(55 µm)



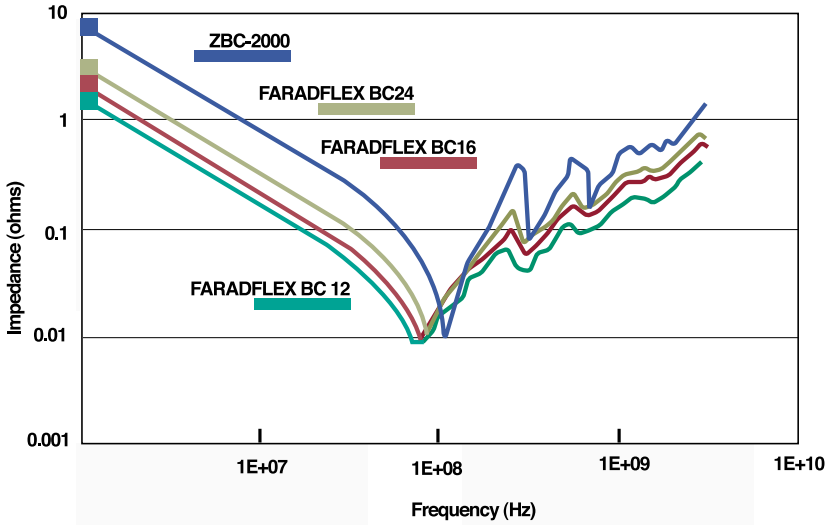
THIN CAPACITOR MATERIAL
FaradFlex™

Buried Capacitance is a trademark of HSCI.

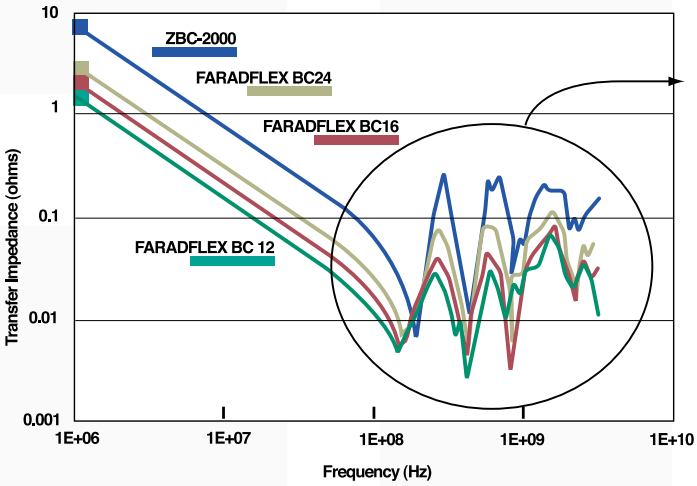
FaradFlex is a trademark of Oak-Mitsui, Inc.

The thin FaradFlex™ layers greatly reduce the Power Distribution Impedance and dampens the Resonance Peaks.

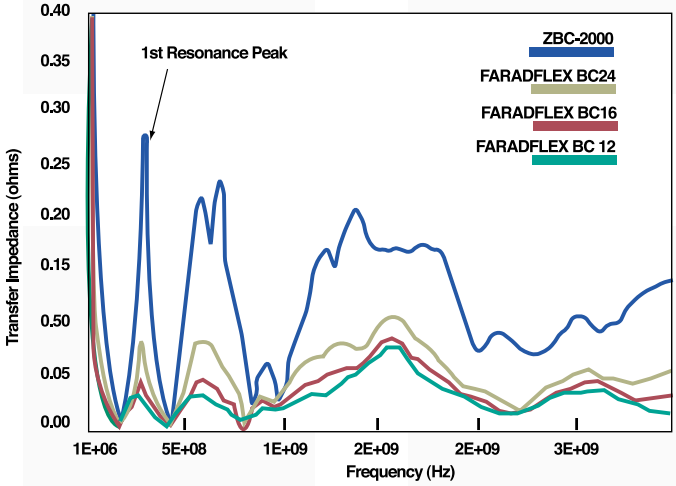
BURIED CAPACITANCE SELF IMPEDANCE



TRANSFER Z PROFILES AT 1" SEPARATION



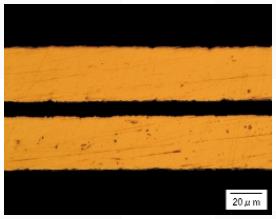
TRANSFER Z HIGH FREQUENCY RESPONSE



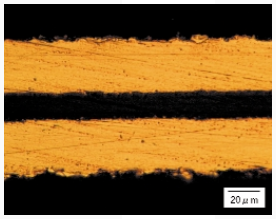
Data Coutesy of Sanmina-SCI Corp.

INNOVATIVE

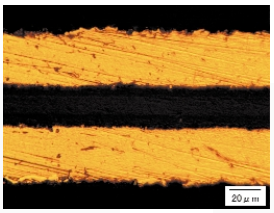
FARADFLEX BC12



FARADFLEX BC16



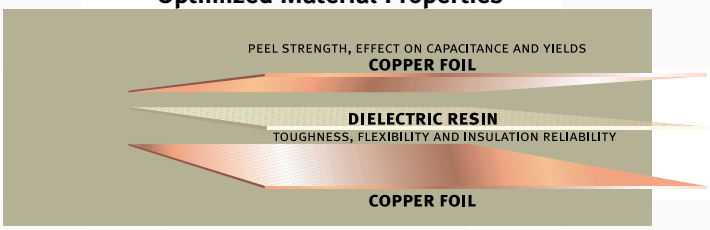
FARADFLEX BC24



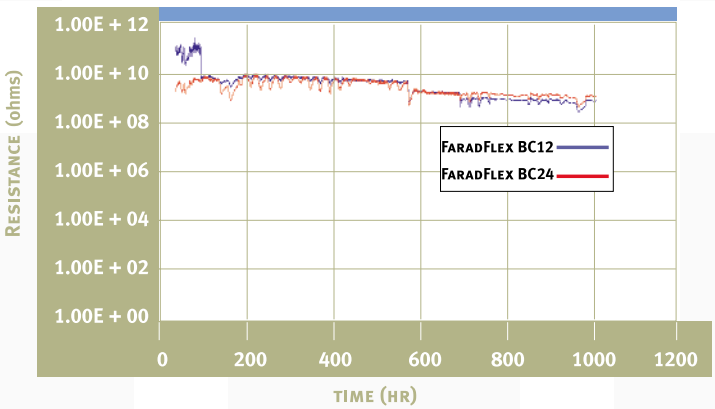
Optimization of the dielectric and proprietary copper foil has resulted in an extremely thin material that not only has excellent electrical properties, but is rugged enough to process through typical PCB inner layer processing. To insure high yields during processing, every core is pre-tested at 500 volts (High Potential)*.

*BC16T is tested at a lower Hi-Pot voltage

Optimized Material Properties



In addition, FARADFLEX™ has been engineered to withstand over 1000 hours during Electro-migration testing.



TEST CONDITION: 85°C/85% 35V

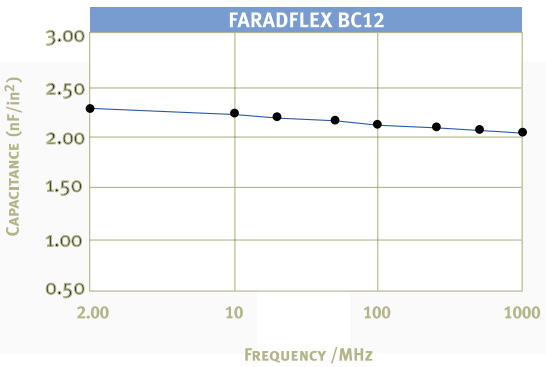


Properties	Methods	FaradFlex					
	IPC or others	BC24	BC16	BC12	BC8	BC12TM	BC16T
Dielectric Thickness, µ	Nominal	24	16	12	8	12	16
Capacitance @ 1MHz, nF/in² (pF/cm²)	IPC TM-650 2.5.5.3	1.0 (155)	1.6 (250)	1.9 (300)	3.1 (480)	4.5 (700)	11.0 (1700)
Dk @ 1MHz	IPC TM-650 2.5.5.3	4.4	4.4	4.4	4.4	10	30
Loss Tangent @ 1MHz	IPC TM-650 2.5.5.3	0.015	0.015	0.015	0.016	0.019	0.019
Peel Strength, lbs/in	IPC TM-650 2.4.9	8	8	8	8	6	6
Dielectric Strength, kV/mil	IPC TM-650 2.5.6.3	5.3	7.3	5	5	6.2	2.8
Tensile Strength, Mpa (kpsi)	ASTM D-882A	152 (22.0)	164 (23.8)	194 (28.2)	126 (18.3)	110 (16.0)	NA
Elongation, %	ASTM D-882A	18.5	16.5	11.5	8.5	6.0	NA
CTE, ppm/°C x-y direction (20-100°C) x-y direction (100-200°C)	TMA	 14 23	 14 23	 14 23	 16 28	 16 38	 NA NA
Boil test, 2hrs boil in water 20 sec dip @ 260C solder (10spec)	–	Pass	Pass	Pass	Pass	Pass	Pass
Thermal Stress (20 sec float @ 288C), times	–	>10	>10	>10	>10	>10	>10
Elec-Migration, 85C/85%RH/DC 35V	–	>1000	>1000	>1000	>1000	TBD	>1000
Flammmability/Temp Rating	UL-94/ UL746	VO 130°C	VO 130°C	VO 130°C	VO 130°C	in process	in process
High Potential (Hi-Pot) Test 500 Volts DC	–	Pass	Pass	Pass	Pass	Pass	*
PWB Processing	–	Both side etching					Sequential lamination

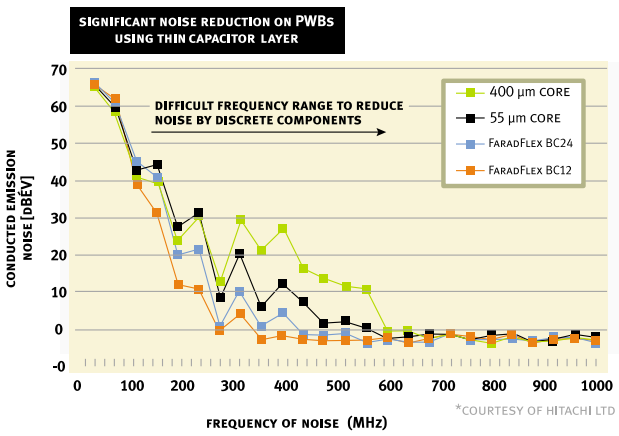
* = BC16T is tested at 100 Volts NA = Not Applicable : Product is not self supporting

This chart provides the typical characteristics for the different products in the FaradFlex™ line of capacitor material.

The capacitance properties are stable over a wide range of frequencies.



FaradFlex™ is also highly effective at reducing power buss noise (due to the thin dielectric).

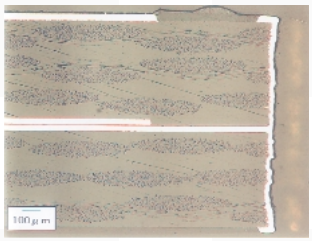


*COURTESY OF HITACHI LTD

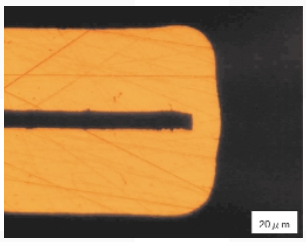


Printed Circuits Boards made with FaradFlex™ layers have demonstrated that no manufacturing process changes are necessary*. The material processes through typical inner layer lines (with the usual procedures for handling thin laminates) and is compatible with standard drilling and plating.

Cross sectional of board made with FaradFlex BC12



Cross sectional after plated - FaradFlex BC12



The FaradFlex™ line of products allows PCB and chip packaging designers to cost effectively improve system performance while saving on expensive board area. Improvements in reliability can also be realized due to the reduced number of solder joints (by removing the discrete capacitors).

To start enjoying the benefits of Buried Capacitance™ technology using the FaradFlex™ line of products, contact the following Oak-Mitsui Technologies representative.

*BC16T may require sequential processing since it is not self supporting.

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