Design and Performance of Polymeric Ultra-thin Substrates For use as Embedded Capacitors: Comparison of Unfilled and Filled Systems with Ferroelectric Particles

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INTRODUCTION

- Review of Buried Capacitance
- Product Design
- Performance Characteristics
- PWB Manufacturing Process
- Impedance/Noise Measurements
- Comparison Summary
- Conclusion

Review

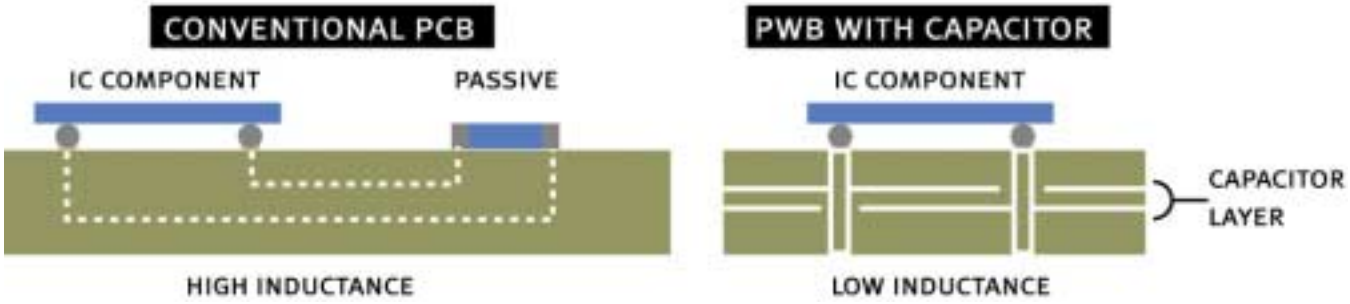
Current applications with Buried Capacitance

Hi-end computers

Network servers

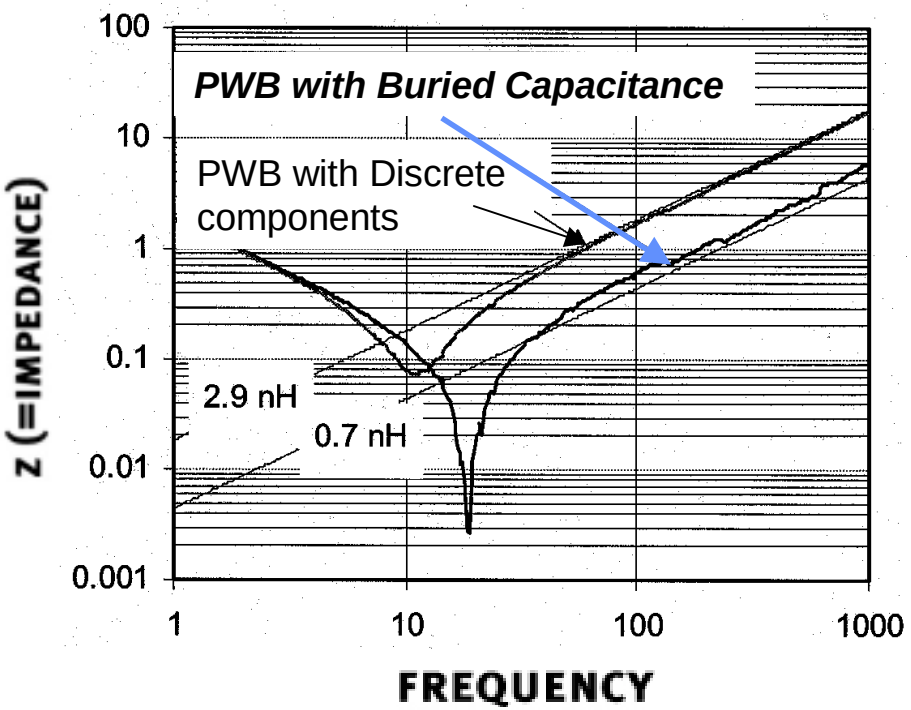
Network routers

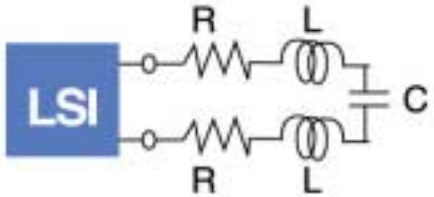
Demand for power distribution system with low impedance



Review

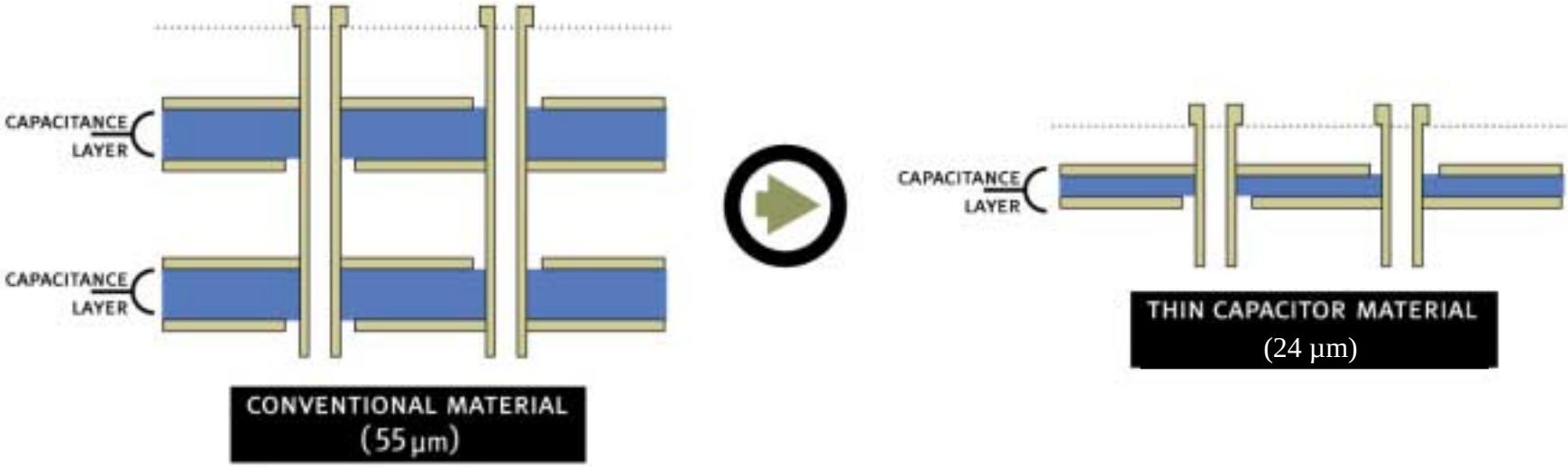
Lower Impedance compared to discrete components





Review

Demand for thin (<25micron) Buried Capacitance



<u>Expectation by using Thin Capacitor Material</u>

- Improvement in Electrical Performance
- Reduce System Cost
- Reduce Thickness of the Board
- Reduce Prototype Revisions

Product Design

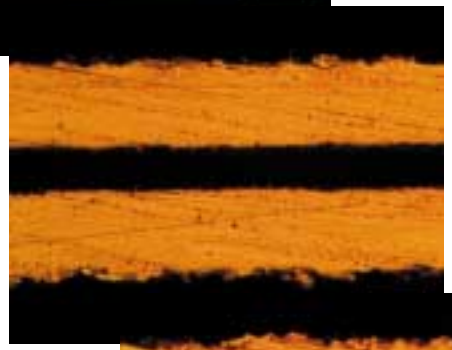
Construction

12 µm



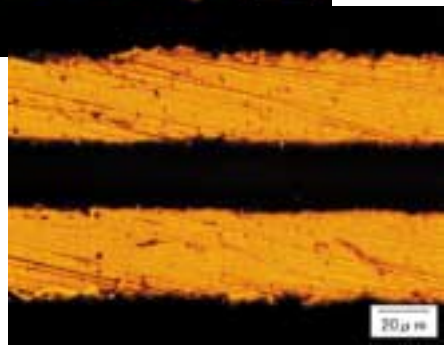
12 micron Polymer Dielectric

16 µm



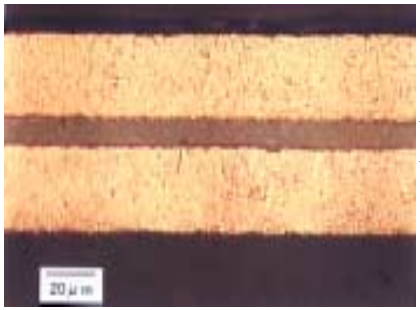
16 micron Polymer Dielectric

24 µm



24 micron Polymer Dielectric

16 µm



16 micron Polymer Dielectric ***with Hi-Dk Filler***

(16 µm with Filler is under development)

-Standard Copper thickness is 35 µm

Product Data

Electrical Properties

Characteristics	Condition	Unit	24µm	16µm	12µm	8µm	16µm-Filler
Capacitance	1GHz	nF/cm^2	0.14	0.23	0.31	0.45	1.75
Dk	1GHz	N/A	4.4	4.4	4.4	4.4	30.0
Df	1GHz	N/A	0.015	0.015	0.015	0.016	0.019
Dielectric Thickness	Nominal	Micro-Meter	24	16	12	8	16

TCC = 95% of X7R

Product Data

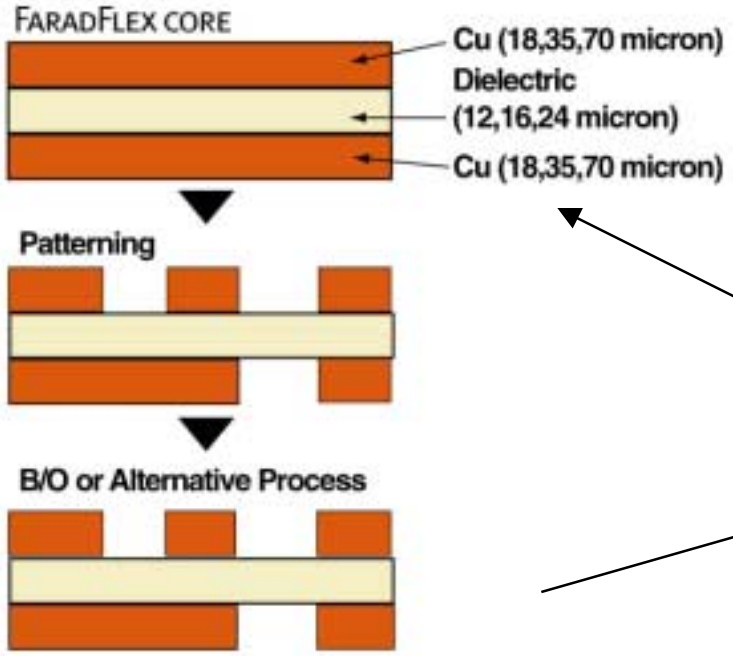
Physical Properties

Characteristics	Condition	Unit	24μm	16μm	8&12μm	16μm-Filler
Tg	DMA	Celsius	200	200	200	200
Peel Strength	As received	lb/in	>8.0	>8.0	>8.0	>6.0
Young's Modules	JIS 2318	GPa	4.8	5.8	7.2	NA
Tensile Strength	JIS 2318	MPa	180	180	180	NA
CTE	IPC TM650	PPM	23/255	23/255	25/270	22/220
Breakdown	1kV/sec	V	>5000	>4000	>4000	>2000
Insulation Reliability	85C/85%/35V	hr	>1000	>1000	>1000	>1000

PWB Manufacturing Process

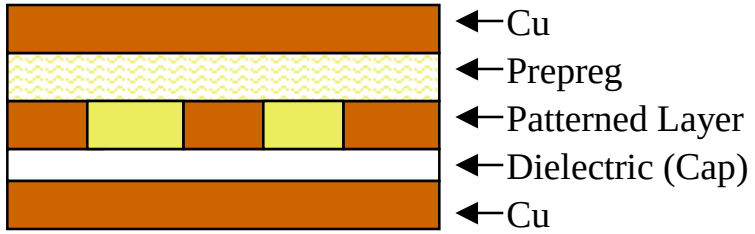
Thin Substrate without Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative



Thin Substrate with Particles

1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative



Subassembly

PWB Manufacturing Process

Summary of Unfilled Substrates

- Substrates Processed at 10 Major PCB Facilities
- Standard I/L Processing
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern
    4. **99+ % Yield** at Hi-Pot (500 Volts)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
- PWBs available from ZBC™ Licensed Fabricators

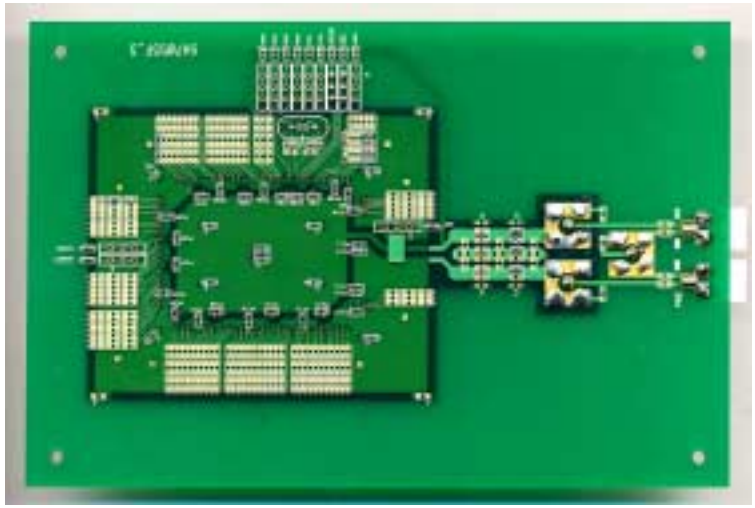
PWB Manufacturing Process

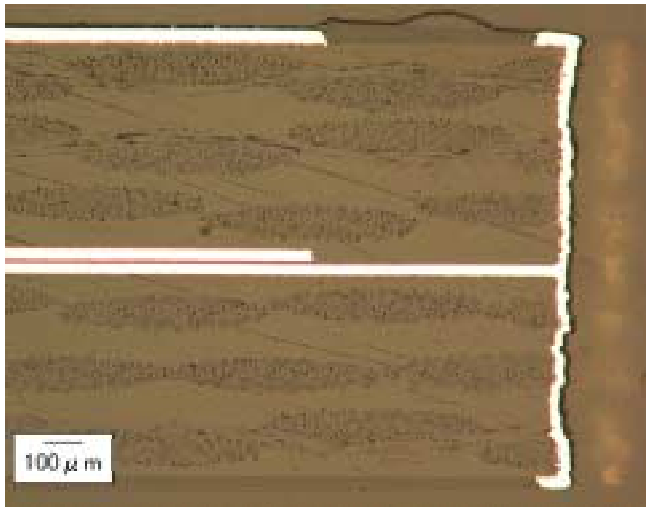
Summary of Filled Substrates

- Substrates Processed at 2 Major PCB Facilities
- Standard I/L Processing with additional steps
- Results
    1. **No loss** due to jams
    2. **No "blow out"** of Clearance holes
    3. **No separation** from border pattern(Cu to edges)
    4. **100 % Yield** at Hi-Pot (100 Volts) (limited quantity)
    5. Both Vertical Racked Black Oxide and Alternative Oxide used **successfully**
    6. Registration between *buried* and outer core layers on subassembly critical
- PWBs available from ZBC™ Licensed Fabricators

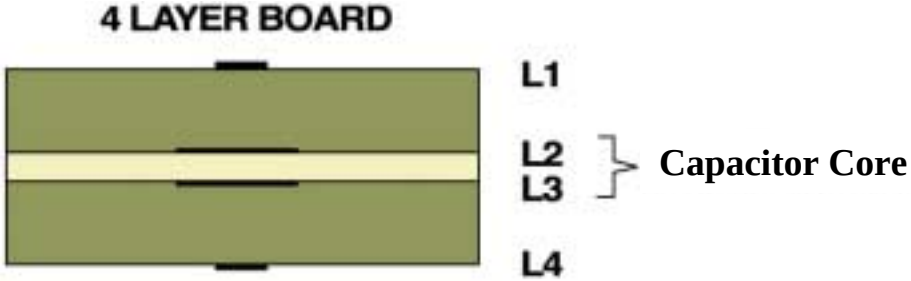
PWB Examples 1

4 Layer Board



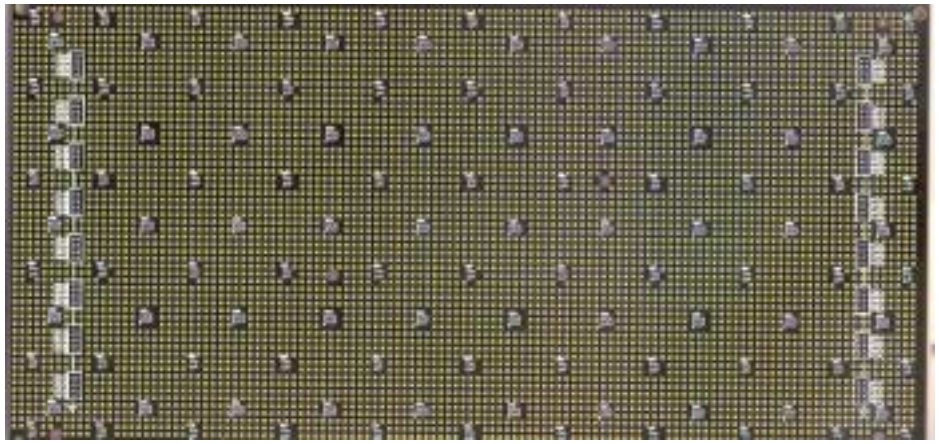


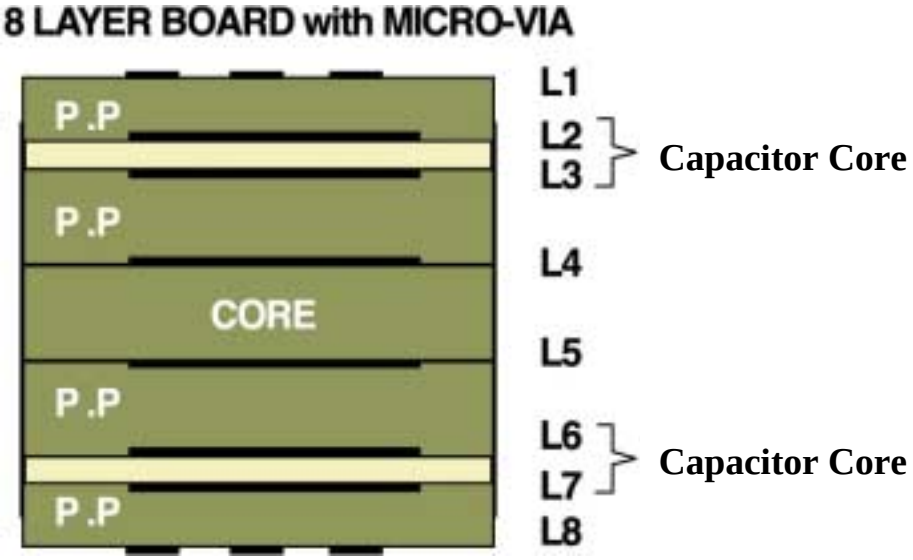
} 12 µm

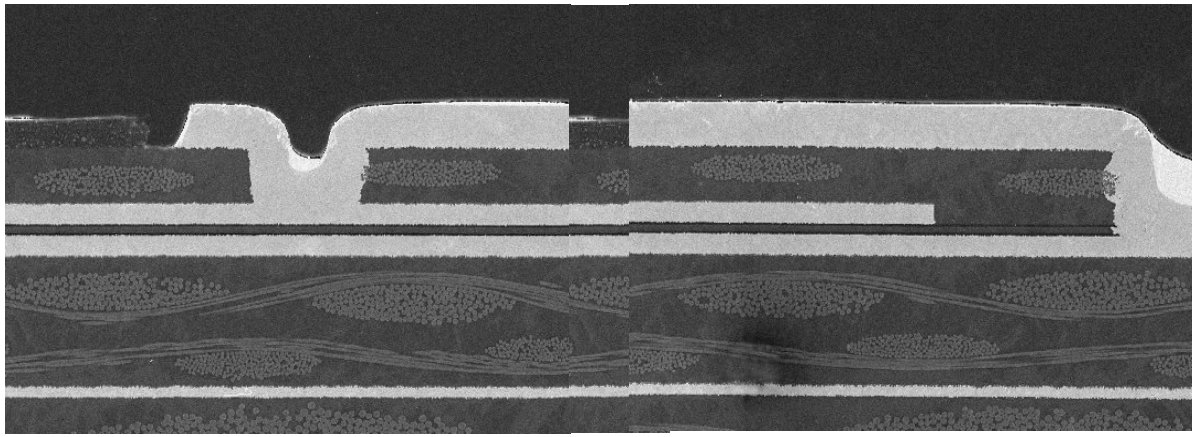


PWB Examples 2

8 Layer Board



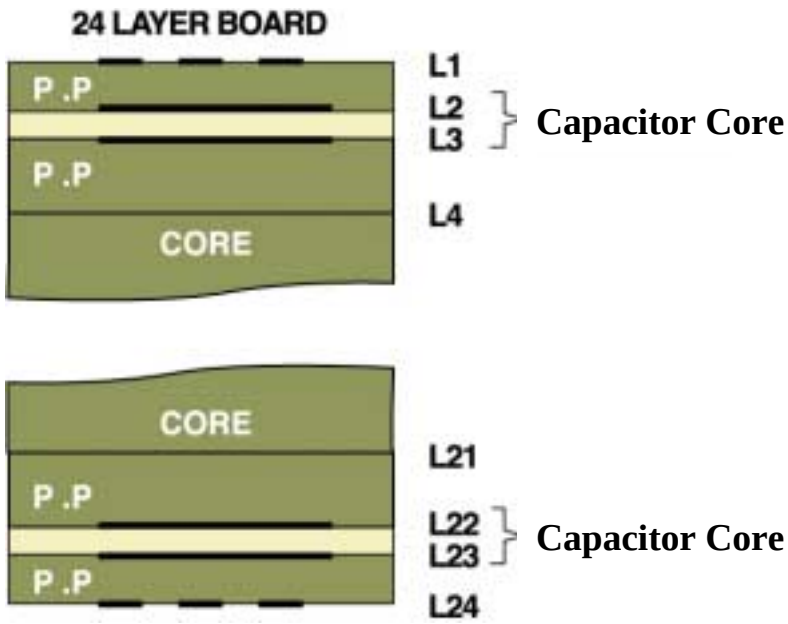


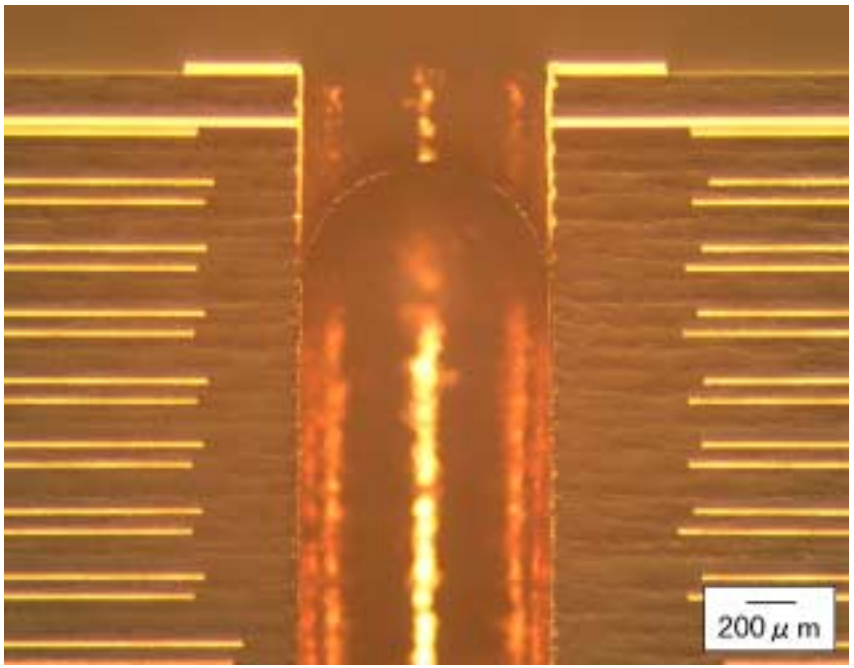


12 µm

PWB Examples 3

24 Layer Board



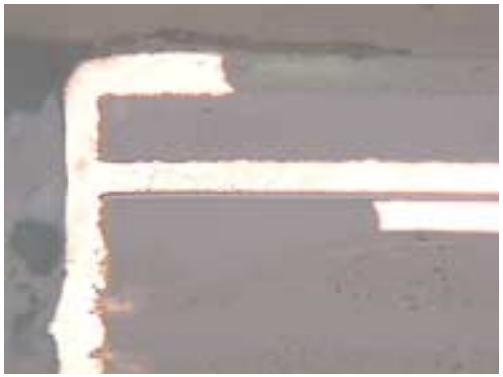


} *12 μm*

Reliability Tests

- Dielectric Withstanding Voltage : 500V Passed, No failure
- T-260 Time to Delamination : 1*2 µm*- 6.3min, *24 µm*- 5.2min
- Blind Via Plating Defects : No defects found
- Thermal Solder Shock (288^{o}C)– 6x : No defects found
- Liquid-Liquid : *24 µm* 4.2%(500 cycle)
- IST Testing: Passed 500 Cycles

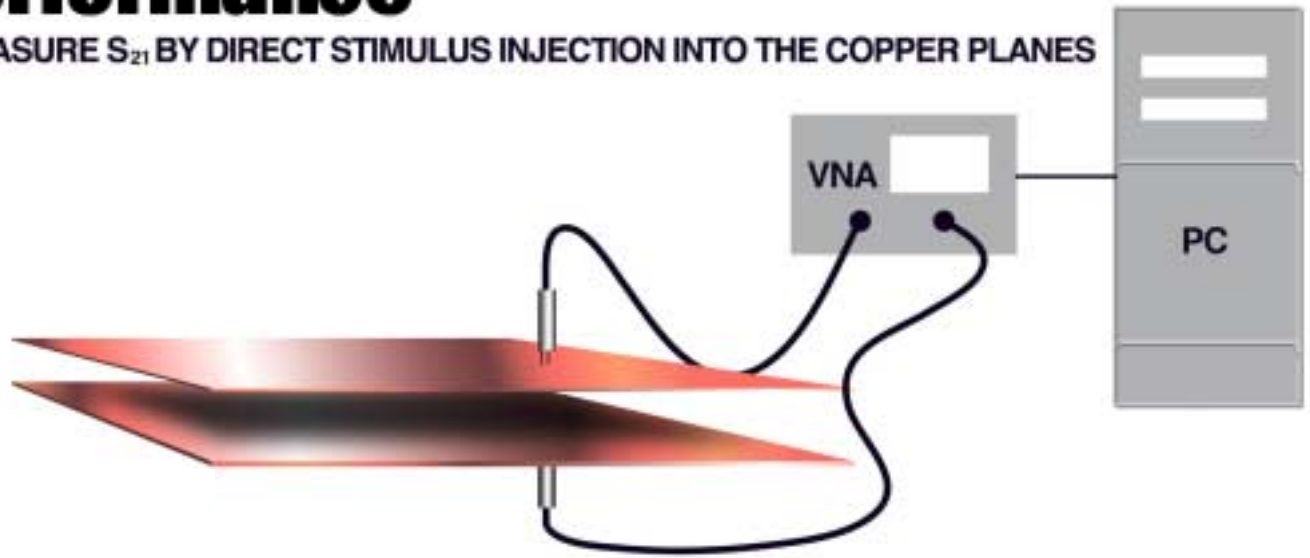
Thermal Solder Shock 288C x6



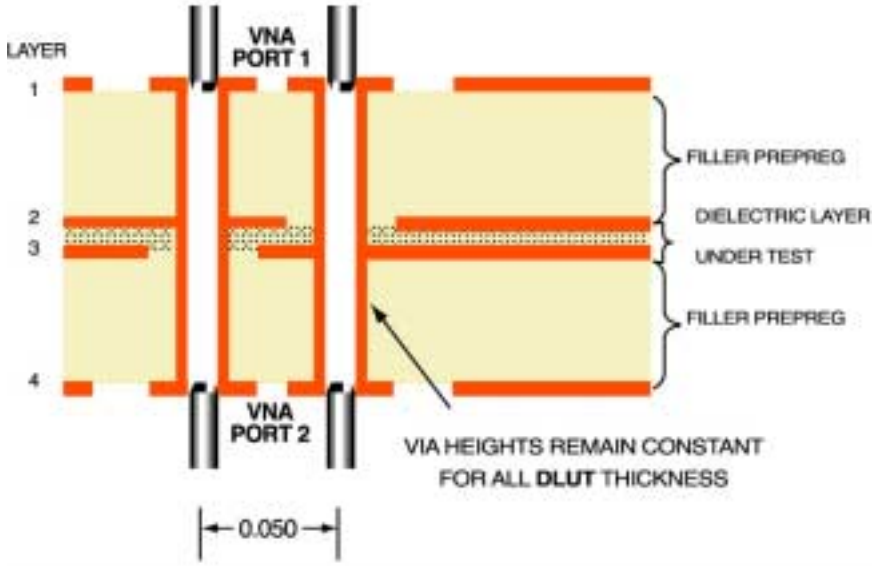
12 µm

PWB Electrical Performance

MEASURE S_{21} BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES

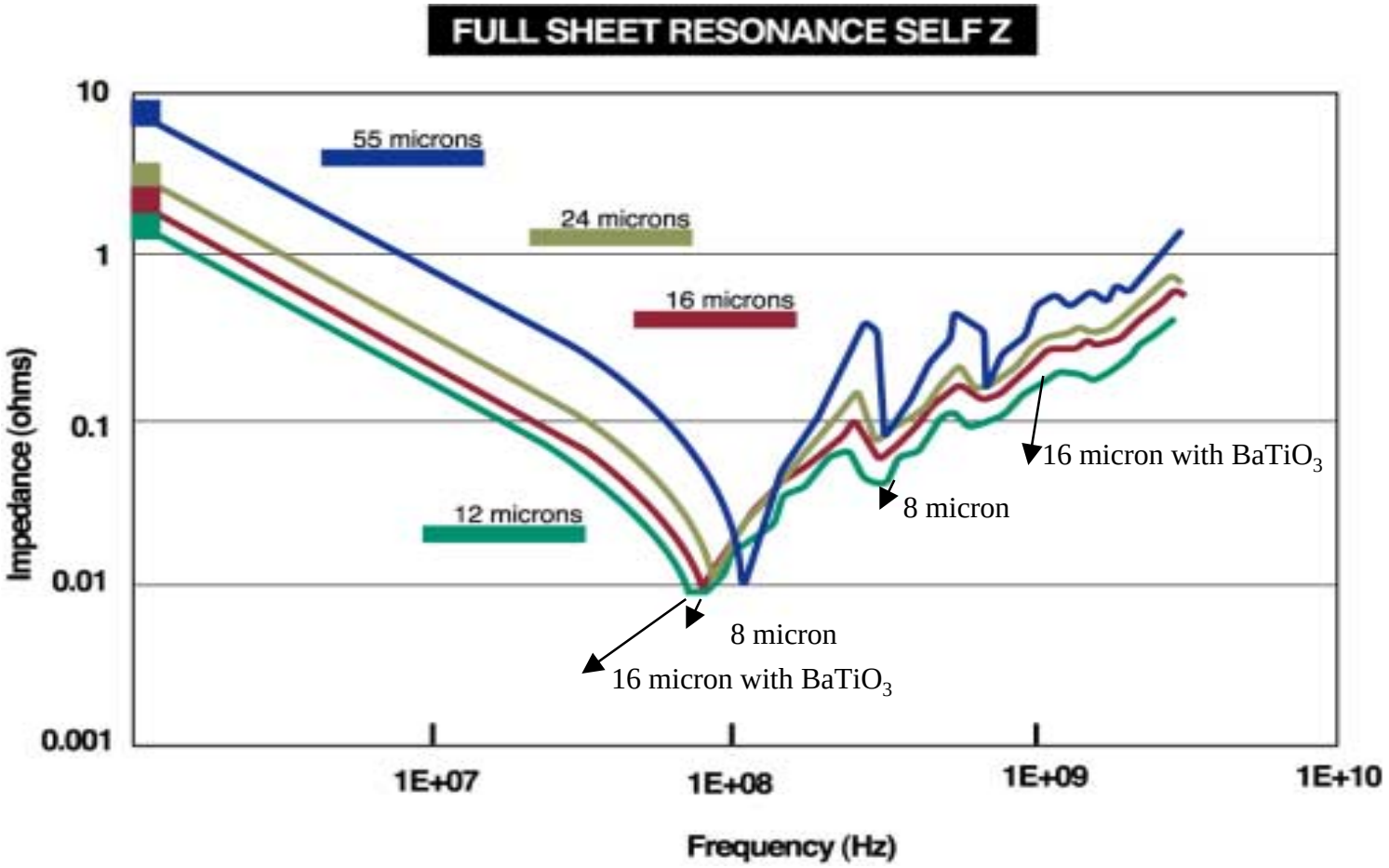


4 LAYER TEST BOARD CROSS SECTION VIEW



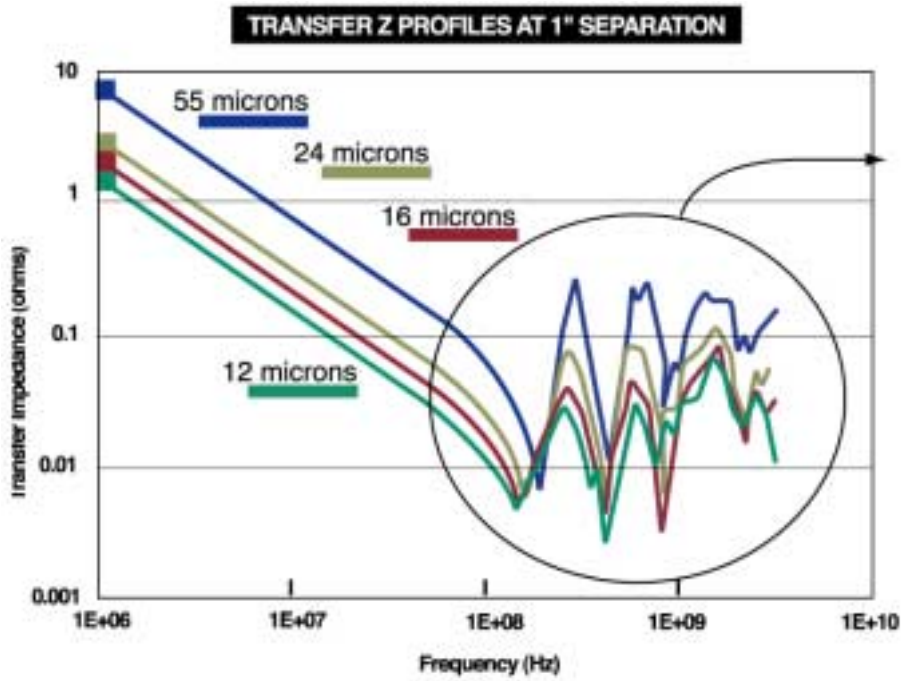
PWB Electrical Performance (Self Z)

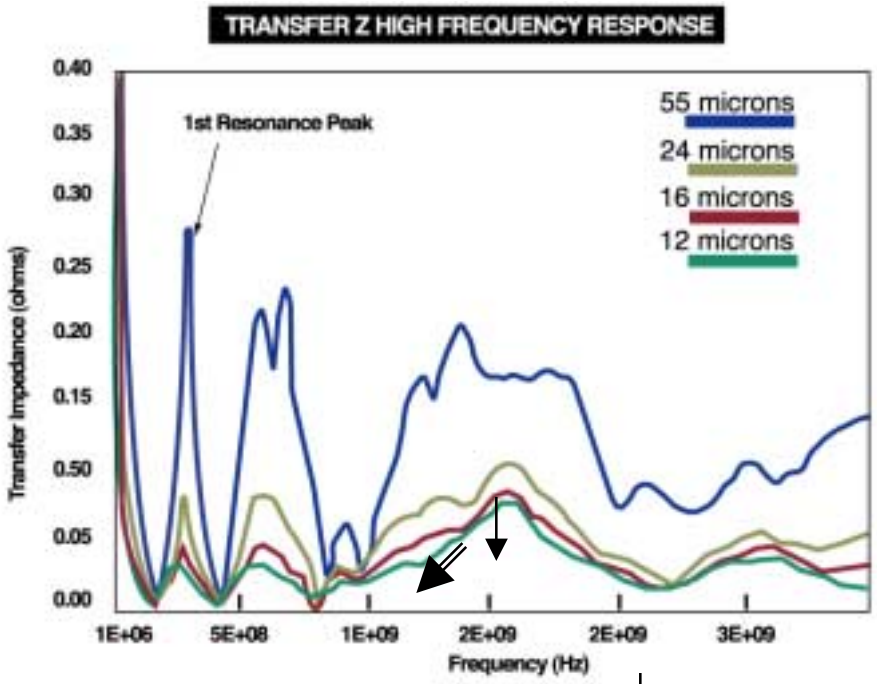
Significant Reduction on Impedance



PWB Electrical Performance (Transfer Z)

Significant Reduction on Impedance





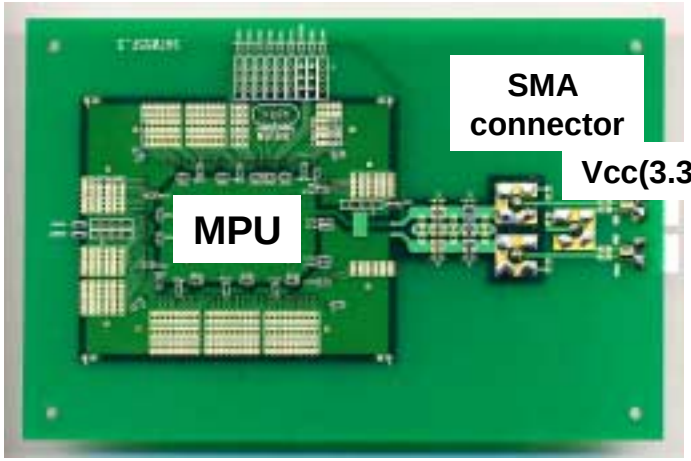
Data Coutesy of Sanmina-SCI Corp.

↓ 8 micron

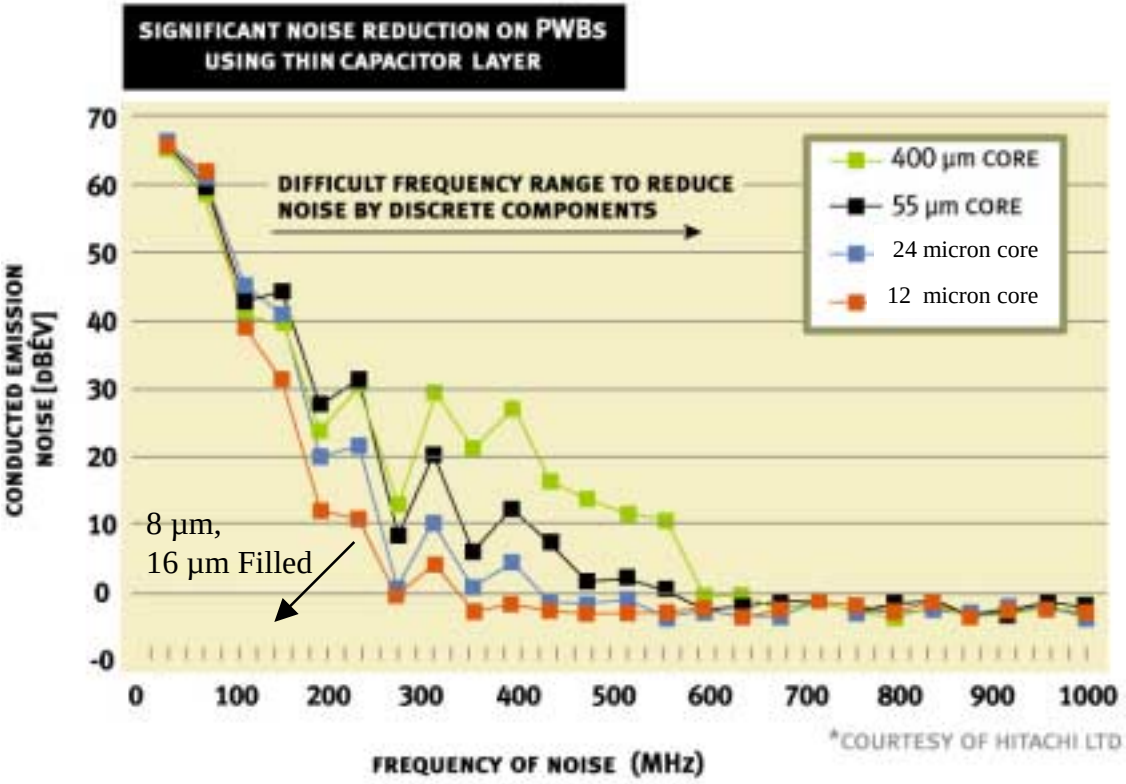
↙ 16 micron with $BaTiO_3$

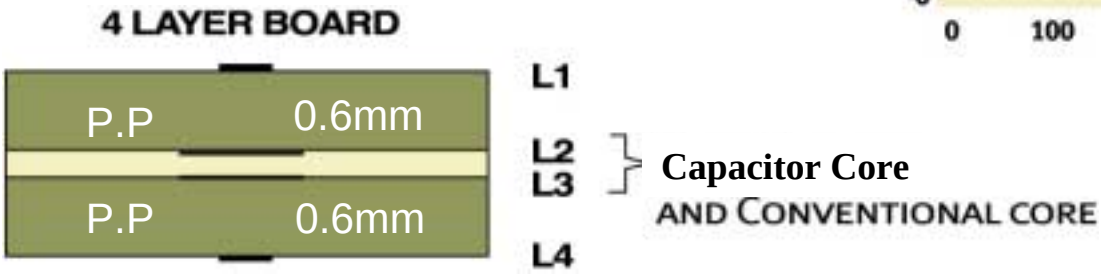
PWB Electrical Performance (Transfer Z)

Significant Reduction of EMI



MPU (40MHz) is mounted on the other side of the board.







Comparison Summary

Unfilled Substrates Versus Filled Substrates

Property	Unfilled Thin Substrates	Filled Substrates
Impedance Reduction/lower noise		+
Electric Strength/ High Potential Testing	+	
Ease of PCB Processing	+	
Cost of Substrate/Raw Board	+	
Cost of Assembled Board	?	?

Conclusion

- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated *excellent* electrical performance and physical properties.
- They are *compatible* with PWB processing; a truly “drop in” material.
- Materials are commercially available from Licensed Fabricators
- The use of Embedded Capacitance can simplify PCB lay-out and reduce the number of prototypes required.
- The Technology can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PWBs
- Additional work is ongoing to
  - Improve PWB manufacturing process of filled substrates