Design and Performance of Ultra-thin Substrates for use as Embedded Capacitors

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Abstract

As CPUs increase in performance, the number of passive components on the surface of the boards are increasing dramatically. To reduce the number of components, as well as improve the electrical performance (i.e. reduce inductance), designers are increasingly embedding capacitive layers in the PCB. The majority of the products in use today utilize reinforced epoxy laminates. These products are relatively easy to handle, provide good electrical performance, but a need exists for even better performance than a fiberglass-reinforced product can produce. Other materials are being developed that are thinner (and thus increase capacitance), but either have problems with dielectric breakdown strength, handling or only marginal improvements over the reinforced epoxy material. A need exists for an ultra-thin (less than 25 micron) material that not only provides improved electrical performance, but can be readily manufactured using standard PCB processing. We will discuss the design criteria we used for developing our family of products, as well as the results. The design of the conductor (copper foil) has been determined to be critical and is examined as well as the dielectric. The products have been through both internal and external testing and are compared to existing and developing capacitor materials. We will describe the electrical as well as the processing characteristics in detail, and how these types of products can greatly improve performance of high-speed systems.

Introduction

The use of thin dielectric substrates to provide Embedded Capacitance has been driven by the need to improve electrical performance of Printed Circuit Boards. Current standard capacitive material used in the industry is mainly the 2mil dielectric thick material, mostly utilized for telecom and networking applications[1)]. For this particular high-end application of PCBs, embedded capacitor technology has been utilized to reduce the inductance between the chip and the power supply. This improves the electrical performance of the distributed capacitance, enhances signal integrity, and reduces impedance at high frequencies while dampen noises.

A number of papers have been published regarding development of materials for embedded capacitors and advantages of incorporating embedded capacitor in PWB. From the electrical performance standpoint, demand is increasing for thinner capacitor material, as low as 10 micron, as the signal frequency increases.[2)]

In this paper, considerations of copper foil and dielectric resin properties (which make up the capacitor material) are discussed. Also, fabrication of the thin film capacitor material incorporating into PWBs and performance of electrical performance using the materials are described.

Investigations

Embedded capacitance materials are constructed from two metal layers (usually copper foils) and dielectric polymer film layer in between. In order to design the construction of the capacitance material, properties of

the copper foil and dielectric layer will be the "keys" to determining the performance of the capacitance materials.

Investigation of the influences of copper foil, dielectric type and dielectric thickness has been conducted to design the construction of the thin capacitance material.

1) Copper Foil

As previously described[3] different types of copper foils were investigated for their influence on the performance of the capacitance material. What we wanted from the foil was not only good performance from the normal characteristics (peel strength, HTE, etc.) but also good capacitance value and insulation resistance.

1-1) Copper Selection Process

We examined four lectro-deposited (ED) and one wrought (rolled) foil. Peel strength, capacitance of the substrate and High Potential (Hi-Pot) Voltage Testing (at 500 Volts DC) were compared. As mentioned in our previous paper[3] it was found that the higher the profile of the copper foil, the higher the peel strength as well as the capacitance values. Unfortunately, increasing the profile also reduced the yield at Hi-Pot testing.

1-2) Copper Foil Decision

When the balance of properties was examined, it was determined that for capacitor material down to 16 micron, a version of reverse treat foil (RTF) gave both good mechanical and electrical performance. For 12 micron material and below a special very low profile (VLP) foil was required.

2) Dielectric Resin

One of the challenges for thin capacitive material is the physical property of the dielectric. The thin dielectric must be tough and flexible in order to withstand processing through PWB manufacturing process. Another challenge for thin dielectric is the insulation reliability, such as hi-pot test and electro-migration.

2-1) Dielectric Selection Process

As indicated previously[3] we looked at two types of unfilled dielectric materials. One type (A) is a conventional and industry standard epoxy resin system. Another type (B) is a proprietary, modified resin system, designed for capacitive material. With these 2 types of dielectric systems, substrates were prepared to evaluate physical properties and insulation reliability.

Resin toughness is an important property to determine the capability to be processed through PWB manufacturing steps. If the resin's toughness were too weak, since the resin thickness is so thin, the resin would break a part during the etching process. As shown in Table 1, resin type B exhibited about 4.5 times higher tensile strength than A, which signifies the advantage of resin type B for endurance during PWB manufacturing process.

Table 1

Resin Type	A	B
Tensile Strength* (N/mm2)	99	448

* Measured on 10 μ m thick resin

2-2) Electro-migration

As the dielectric layer thinner, there is a concern regarding insulation reliability between the layers. Electro-migration tests were conducted at the condition of 85C/85%/35V, for two different resin systems. The dielectric thickness was prepared at 10 μ m. The result is shown in Table 2.

Although resin type A lasted only 682 hours before electrically shorted, resin type B lasted for over 1000 hours. The differences in ion contamination, moisture absorption and polymer structure seems to be influencing the electro-migration endurance period.

Table 2 Electro migration test

Resin type	Lasted hours		
	N=1	N=2	Avg.
A	658	706	682
B	>1000	>1000	>1000

2-3) Dielectric Decision

Based on the above results it is obvious that resin B is the best option for the dielectric material.

Description of the thin capacitance material

Based on the investigations of copper foil and dielectric resin properties, suitable copper foil and resin type was selected to construct/manufacture 12, 16 and 24 μ m dielectric thickness capacitive material. Characteristics of the developed capacitive materials are listed in Table 3.

Table 3 – Dielectric material characteristics

Properties	24 μ m	16 μ m	12 μ m
Copper foil type	RTF	RTF	VLP

Dielectric type	B	B	B
Copper weight (oz)	1	1	1
Peel strength (kN/m)	>1.0	>1.0	>1.0
Dielectric thickness µm	24	16	12
Capacitance at 1GHz nF/cm^2	0.14	0.23	0.31
Dk at 1GHz	4.6	4.6	4.6
Df at 1GHz	0.012	0.012	0.012
Dielectric breakdown V	>500	>500	>500
Tg(DMA) Celsius	>200	>200	>200
Electrical migration*(hrs)	>1000	>1000	>1000
Solder float (288Cx5times)	Passed	Passed	Passed

*RH85%/85C/35V

Processing of the capacitance material

Three different PCB fabrication facilities have processed the substrates. The trials were conducted on thin film capacitance materials of 24, 16 and 12 µm dielectric thickness, to see the capability of processing the material with existing conventional manufacturing equipment.

1) Pattern formation

One of the major design criteria for the material was to be able to be processed through the standard inner layer process. The typical process consists of:

1. Chemical Pre-clean
2. Dry Film lamination
3. Image Expose
4. Develop, Etch and Strip (Dual sides)
5. Black oxide or Alternative

Due to the tough and flexible nature of the resin, the material was processed without being damaged. This included not having the clearance holes "blow out" during etching or having the border detach from the circuit. This is not the case for many thin capacitor materials.

Although, processing thin capacitance material can be challenging and may need modifications or adjustment to the process, the material was capable of processing through the conventional PCB manufacturing steps. This was proven at all three fabrication facilies.

2) Hi-Pot(High potential) test

The patterned laminate was tested to Hi-Pot test. All the panels passed the 500V test, including the 12 micron dielectric thickness material. The high yields at inner-layer test are due not only to the construction of the material, but by having any marginal material caught at the substrate manufacturer by pre-testing.

3) Lamination

Scaling is a very important parameter for multilayer lamination. Figure 1 shows the measured result of the movements of the distance between the holes during the process. As it can be seen, thin capacitance material's movement was equivalent to that of 50 μ m (2mil) core material. This is most likely due to the fact that since most of the copper is retained, the dielectric thickness has little effect on the scaling. Hence, as a first trial the scaling factor for the thin capacitance material can be the same as is used for the 50 μ m core material. This was verified at the three PCB facilities previously mentioned.

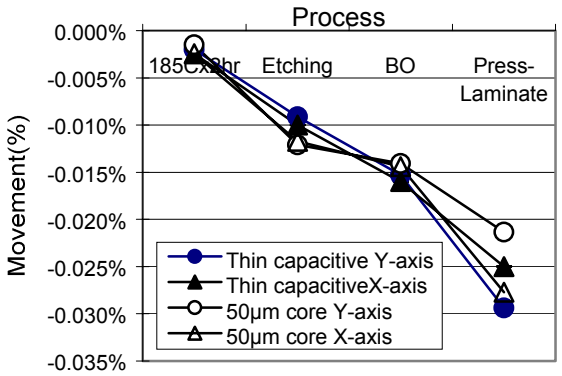


Figure 1 – Dimensional stability during the process

4) Through hole and micro-via plating reliability

Figure 2-4 shows the cross-sections of the boards using thin capacitive material. Figure 2 is the cross-section of a PTH in a board using 12 μ m dielectric thickness capacitor material and Figure 3 is of a 24 μ m capacitor board connected with a micro-via. Because the material is non-woven, it is easily laser ablated and plated. Figure 4 is of a 24 layer board using the 12 micron material after 6x Solder shock at 288^{0}C. Good connection of the plated copper to the thin dielectric layers is observed. Also, all the cross-sections show good compatibility with the surrounding FR-4 laminates.

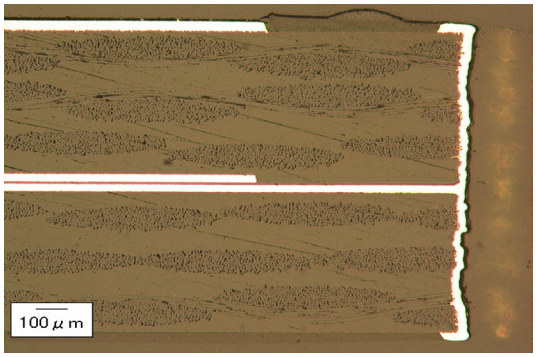


Figure 2 – Cross-section of board using 12 μ m capacitance layer

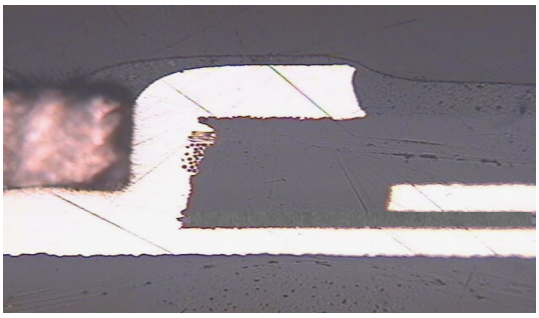


Figure 3 – Cross-section of board using 24 μ m capacitance layer with Micro-via

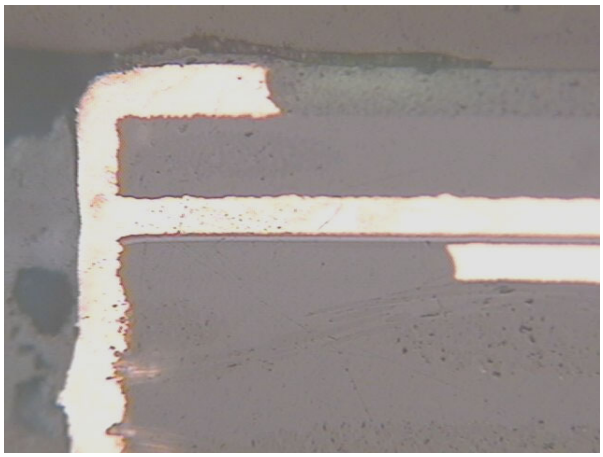


Figure 4 – Cross-section of 24 layer board using 12 μ m capacitance layer after 6x Solder Shock

Electrical performance of the board using thin capacitive material

Many advantages on electrical performance, such as power distribution and Electro Magnetic Interference (EMI), can be expected by using thin capacitive material in PWB.

Conducted emissions on the supply line for a microprocessor (MPU) running at 40MHz were measured by VDE method. No discrete decoupling capacitors were mounted on the four-layer board (See Figure 5). Comparison of conducted emissions between conventional standard 400μm laminate core and 10μm thin film capacitive core are shown In the Figure 6. Significant reduction of emissions in the frequency range of 150 to 550MHz, which is known as the difficult range to reduce by discrete capacitors were observed by the thin film capacitive core. Lower effective inductance and larger capacitance of the thin film core structure improves performance of supply decoupling for MCUs.

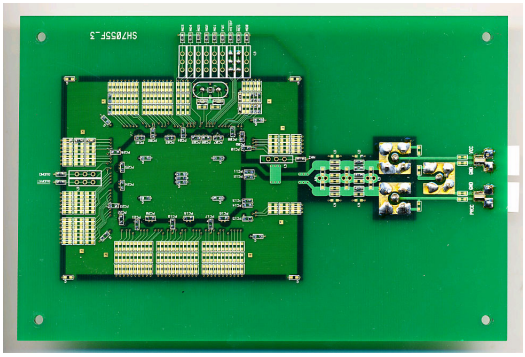


Figure 5 – Board used for the noise current measurement [4)]

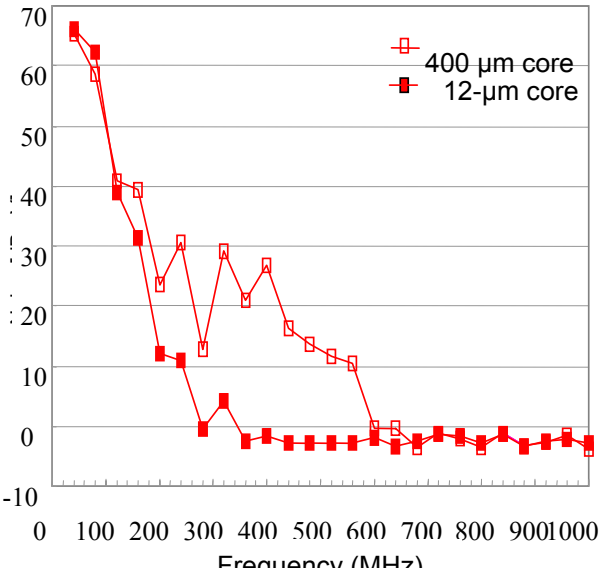
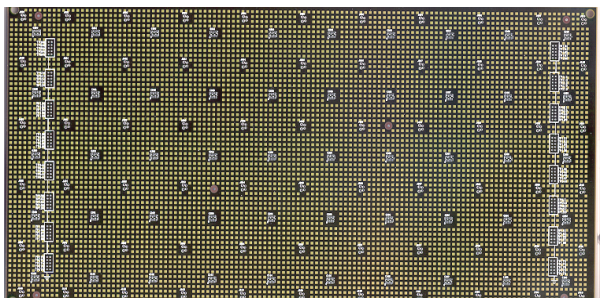


Figure 6 – Comparison of noise current with standard laminate core and 10 μm core [5)]

The reduction in EMI is a good benefit of using these thin capacitor substrates, but the major benefit is in the



reduction in impedance of the power planes. Figure 7 shows the test vehicle used to check the power plane impedance. Figure 8 shows the reduction in self-impedance of various capacitive layers. Figure 9 shows the transfer impedance change in capacitance at 1" distance. The distance from the chip and the shape of the planes will impact these numbers, but it is easily seen that the thinner the material the lower the impedance. This is a very important design consideration and shows the benefit of the embedded capacitor material.

Figure 7- Test Vehicle for measuring power plane impedance.

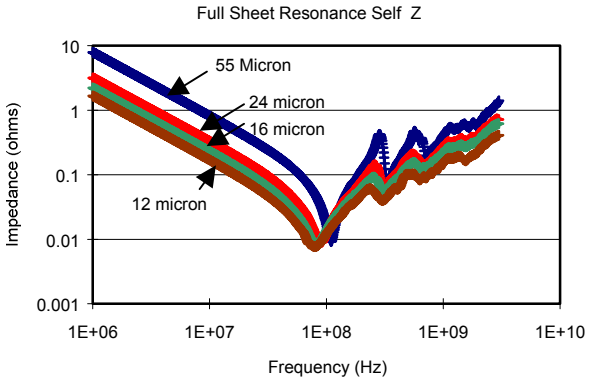


Figure 8- Self Impedance Results

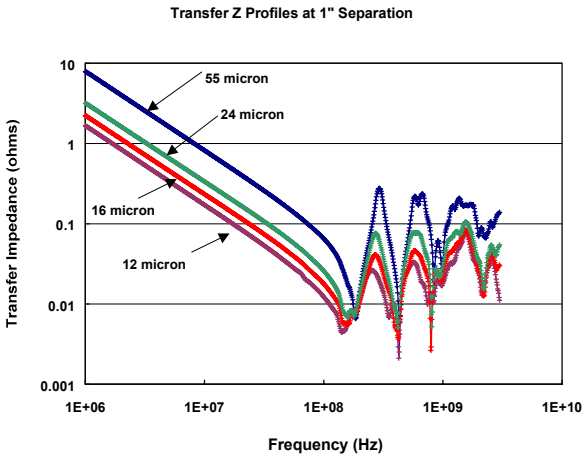


Figure 9- Transfer Impedance Results

Conclusion

Contributions and influences of copper foil and dielectric resin properties to construct a thin dielectric capacitive material have been investigated.

Suitable copper foil type and dielectric resin was selected to construct thin film capacitive material.

The thin film capacitive materials, 12, 16 and 24 micron dielectric thickness, were capable of processing through the conventional PWB manufacturing steps. This was shown at multiple PCB shop locations.

The electrical performance and capacitance values are improved over the traditional FR4 laminate substrates. The ability to withstand 500 volt Hi-Pot testing (even at 10µm) is significant, and has not been demonstrated by any other thin polymer capacitive substrate. A dramatic reduction in EMI and both self and transfer impedance will allow for better system performance especially at high speeds. This will also help to simplify the designer's tasks.

We are continuing to work on driving the thickness even lower. Work on both the foil and dielectric are needed to make this a reality. Also, we are developing a ceramic loaded substrate for use as a replacement for discrete capacitors on daughter cards and chip packages.

As the demand for a power distribution system with low impedance and control of EMI increases for hi-end computing boards with high signal frequency, the usage of thin film capacitive material in PCBs is expected to grow.

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5) Courtesy of HITACHI LTD.